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# A Logic CMOS Process Compatible Two-Bit MTP SONOS Nonvolatile Memory

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**Abstract-** A novel MTP (Multi-Time-Programming) flash memory with an effective shrinking of the storage node size and physically isolated 2 bits has been proposed. It was made by a pure CMOS logic compatible process without additional mask. By carefully chosen proper operation schemes, reliable data retention can be reached. First, testing of this MTP cell by the conventional Channel-Hot Electron Injection (CHEI) programming scheme, huge charge loss was observed as a result of the mismatch between electrons and holes. Therefore, a Forward-Bias Electron Injection (FBEI) scheme was suggested for the programming to prevent the charge loss and allowed up to $10^4$ P/E cycles for multi-time programming purpose. The 2-bit operation was also demonstrated with larger operation window comparing to that of CHEI.

## 1. Introduction

In recent years, two major solutions of the nitride storage have been considered for embedded applications, i.e., conventional SONOS [1] or OTP(One-Time-Programming) [2-3]. For the latter, using a logic compatible process with a low-cost and flexible design for micro-controller, smart card, RFID, mobile applications, makes it more attractive comparing to the conventional SONOS. Although OTP with a select transistor for programming or erase provides certain advantage, it requires *two transistors for one-bit*. On the other hand, there is a demand in increasing the cell density or providing the MTP(Multi-Time-Program) capability [4]. In this regard, we will propose a simple cell design without the need of extra mask and a simple ONO process *based on a pure CMOS logic process*. In this paper, a new structure of MTP cell by using a self-aligned process to form nitride storage nodes will be proposed. It provides certain advantages such as, 2-bit operation, programming/erase capability as SONOS, good retention, and more importantly the process simplicity.

## 2. Device Preparation

The novel n-channel MTP SONOS with ONO thickness (60/80/60) ($A^o$), were fabricated using standard CMOS technology. Cell area with $L_{eff}$= 0.19um and $W_{mask}$= 0.24um was used. The two bits are physically isolated as shown in Fig. 1(a) and storage node size is 50nm, where the major process flow is shown in Fig. 1(b).

## 3. Results and Discussion

***A. The operation schemes:*** First, the conventional schemes using CHEI for the programming and BBHHI (Band-to-Band Hot Hole Injection) for the erase are used for the cell operation. Figs. 2(a) and (b) show their transient characteristics respectively. However, the programming speed is slow in the msec range for achieving a $V_{th}$ window of 3V. A good scheme, proposed by us before in [5], FBEI (Forward Bias Electron Injection), Fig. 3, was used here. During the electron emitting phase $T_1$, the substrate-drain junction is forward biased and electrons are injected into the substrate. Subsequently, the junction was reverse biased at phase $T_2$, which will cause the previously generated electrons in the substrate to be accelerated across the depletion region and injected into the gate dielectric. Figs. 4(a), (b) demonstrates the way to find the optimum conditions for the programming. Then, in Fig. 4(c), at the same 3V $V_{th}$ window, the cell can be improved with a three-order faster speed in the usec range.

**B. *Endurance and retention for one bit operation:*** The endurance characteristics with CHEI programming and BBHHI erasing are given in Fig. 5 (a). At first, the $V_{th}$ increases dramatically, while the $V_{th}$ window saturates at 2V after 200 program/erase cycles. In comparison, from Fig. 5(b), by using the FBEI scheme, not only the window closure is eliminated but also a wider operation window (~2.5V) can be achieved. Fig. 6 shows the comparison of the data retention between the two different schemes, CHEI versus FBEI. Data retention in a 10-year lifetime prediction gives a much larger window for FBEI compared to the CHEI ones. To understand why the FBEI exhibits much better data retention than the CHEI one, the charge profiling was elaborated as follows. Figs. 7(a) and 7(b) shows the measured charge pumping currents for the cell before and after the programming. Based on these two figures, the charge profiles can be calculated [6]. In Fig. 8, it shows the calculated charge profiles before and after the programming operation, in which the peak of FBEI is found to be closer to the gate edge of the drain region. This is because the difference of physical schemes in that the injection in FBEI is occurred inside the drain region, while CHEI is located at the drain-bulk junction. This provides the advantage of better electron-hole mismatch in the FBEI scheme during the cell operation.

***C. Examination of the charge distribution:*** To maintain a good mismatch and prevent the charge loss, the electrons (during the programming) and holes (during erase) needs to be more close to each other [7]. For the two different schemes (CHEI and FBEI), the mismatch can be illustrated by the gated-diode measurement [8] in Fig. 9, where the location of FBEI is away from the channel region such that electrons will be easy to recombine with the holes during BBHHI erase. Tables 1 and 2 shows the steps to calculate the remaining charges, represented by area ΔA, which represents the recombined charge amount before and after the P/E cycles. Fig. 10 is used to explain why FBEI has such a higher efficiency. This leads to the conclusion that FBEI shows much higher electron-hole recombination efficiency as well as a decreasing charge loss in the lateral direction.

*D.* ***Two-bit per cell operation:*** Fig. 11 (a) is the endurance of two-bit operation by CHEI. Fig. 11 (b) shows endurance of two-bit operation by FBEI. It reveals that the window of the 2nd bit is narrower due to the interference from the 1st bit in CHEI scheme. While for FBEI scheme, a large 2.5V window can be maintained after P/E cycling. Figs. 12 (a) and (b) are the comparison of data retention for two schemes, in which a much larger window can be achieved for FBEI scheme from this 10-year lifetime prediction.

In summary, a very promising 2-bit MTP cell without the need of extra mask and the select transistor has been proposed. The concept of MTP is to design a cell with *multi-programming capability* better than OTP, while the endurance (up to $10^3$ or $10^4$ cycles) does not need to compete with conventional SONOS. This cell meets this requirement and is compatible with the CMOS logic process such that it is suitable for embedded applications. By using a unique FBEI scheme, much better reliability can be achieved. In other words, for two-bit operation, FBEI has better endurance and data retention than CHEI ones because the second bit interference can be prevented.

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**References:**

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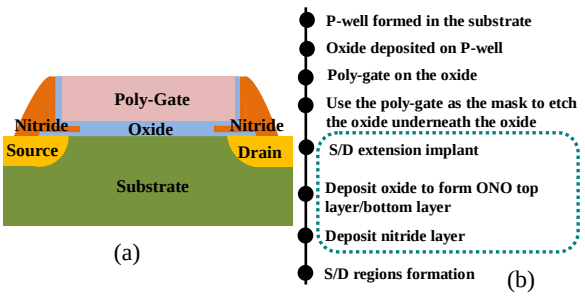


**Fig. 1 (a)** The structure of MTP formed by etching the oxide underneath the poly gate, and form ONO layers as the storage node. (b) The process flow of an n-channel MTP SONOS.

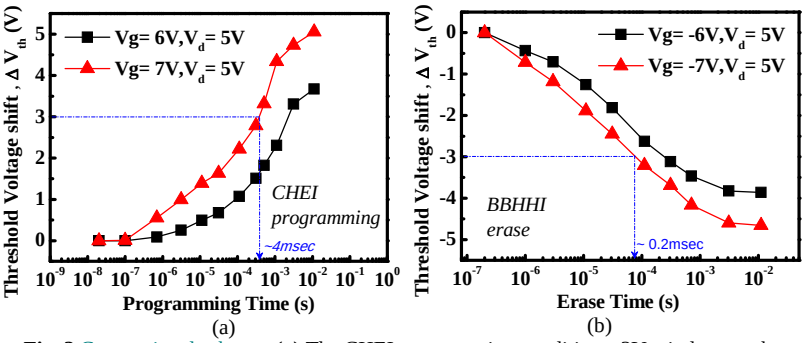


**Fig. 3** Conventional scheme: **(a)** The CHEI programming conditions; 3V window can be achieved by Vg= 7V, $V_d$= 5V and pulse duration T= 200us. **(b)** The BBHHI erasing conditions; 3V window can be obtained at Vg= -7V, $V_d$= -5V and T= 100us.

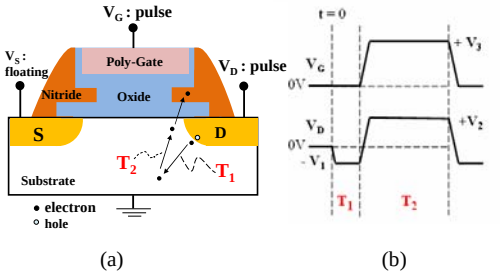


**Fig. 2 (a)** Experimental set up and **(b)** timing diagram of FBEI scheme (programming).

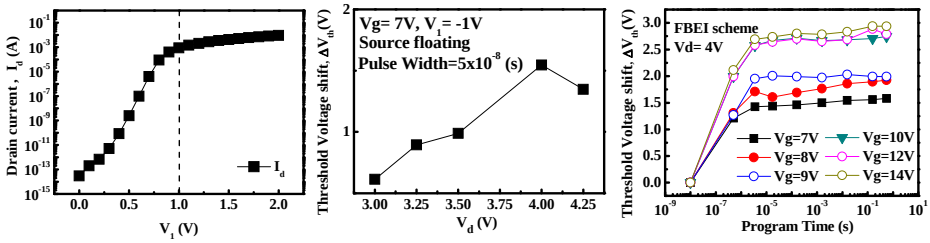


**Fig. 4** The steps to determine the pulse conditions of FBEI scheme: **(a)** By varying the emitting voltage at $T_1$ to find the best bias condition for the programming. **(b)** By varying the drain bias at $T_2$ to find the best condition for $V_2$. **(c)** Changing the gate voltage at $T_2$ to find the best condition for V3.

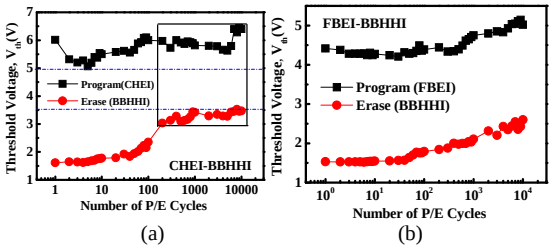


**Fig. 5 (a)** The endurance characteristics by conventional CHEI programming and BBHHI erase. **(b)** Window closure can be prevented while keeping a good window(~2.5V) using the combination of FBEI programming and BBHHI erase.

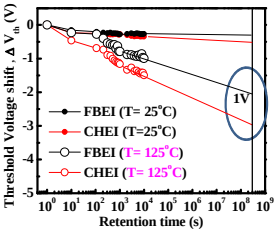


**Fig. 6** Data retention test at various temperatures. The data retention of FBEI programming is 1V better than that of CHEI at T= 125°C.

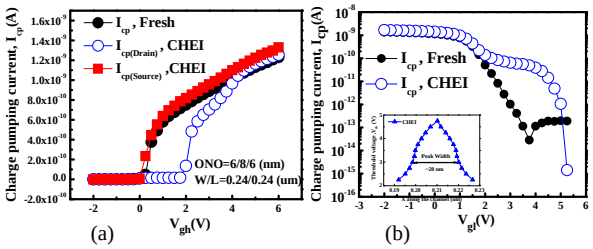


**Fig. 7** Charge pumping measurement using **(a)** fixed base **(b)** fixed top methods to determine the charge distributions after the program.

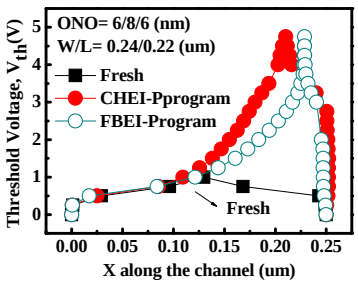


**Fig. 8** Results of the injected charge profiles. The location of the FBEI injected charges is farther into the drain region comparing to the CHEI ones.

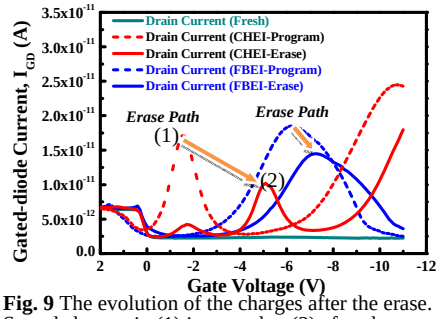


**Fig. 9** The evolution of the charges after the erase. Stored charges in (1) is moved to (2) after the erase. The erase path of FBEI manifests that FBEI-injected charges are more closer to the BBHHI-injected holes.

$$A \propto Q = \int_0^{\infty} I_{GD} dV_G$$

A : the area under the measured $I_{GD}$-$V_G$ curve
Q : total charges in nitride

$$\Delta A = \int_0^{\infty} I_{GD} dV_G \,|_{program} - \int_0^{\infty} I_{GD} dV_G \,|_{erase}$$

ΔA ∝ the net amount of electrons which are recombined by injected holes

≡ Erase efficiency

**Table 1** The equations to calculate the erase efficiency. Erase efficiency is defined as the amount of electrons which are recombined with injected holes.

| schemes | A | ΔA |
|---|---|---|
| CHEI (program) | 2.26E-11 | 7.97E-12 |
| CHEI (erase) | 1.46E-11 | |
| FBEI (program) | 6.49E-11 | 1.50E-11 |
| FBEI (erase) | 4.99E-11 | |
| △A(FBEI) = 1.89△A (CHEI) | | |

**Table 2** The comparison of the erase efficiency between CHEI and FBEI. FBEI is 1.89 times higher than CHEI.

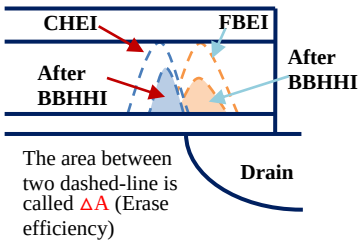


**Fig. 10** The electron distributions in the nitride layer after program/erase. The distribution of FBEI is deeper into the drain side than that of CHEI. Also, the shaded area is smaller for FBEI and BBHHI combination, meaning that mismatch can be improved.

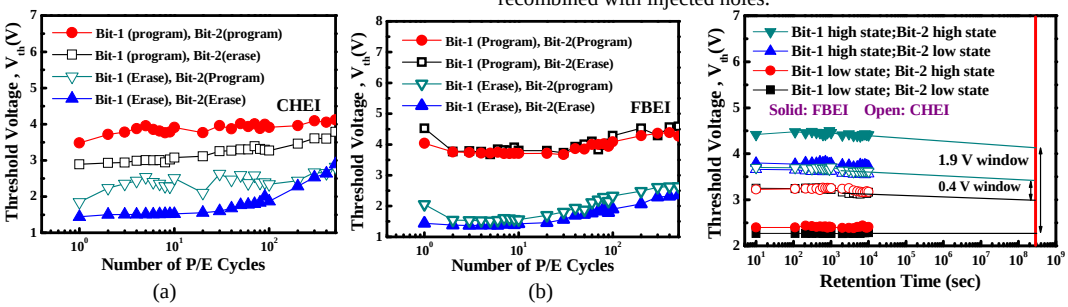


**Fig. 11** Endurance for 2-bit operation: **(a)** The window closure of 2-bit/cell operation in CHEI is serious because of the electron-hole mismatch. Also, the two bits are not-balanced. **(b)** A 2.5V window can be maintained by the FBEI scheme after long term P/E cycling in the FBEI scheme.




**Fig. 12** The comparison of data retention for 2 schemes. For 10 years lifetime prediction, FBEI still kept a 1.9V window, while CHEI was down to 0.4V window.