Investigation of Random Grain-Boundary Induced Variability for Stackable NAND Flash Using 3D Voronoi Grain Patterns

Ching-Wei Yang and Pin Su
Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan
Email: oranfrog.eecs96@g2.nctu.edu.tw, pinsu@faculty.nctu.edu.tw

Abstract
We investigate the random grain boundaries (GBs) induced variability in poly-Si thin film transistor (TFT) using 3D Voronoi grain patterns. Compared with the 1D and 2D methods, the 3D Voronoi grain can show a more realistic variability when devices are downcaled along the channel height (H_{ch}) direction. Our study indicates that a full 3D consideration is needed when modeling the random GB induced variation.

I. Introduction
Building 3D structures is one way to pursue higher data storage density in NAND flash memories [1]. Since most of these multi-layered structures adopt poly-Si channels which may exhibit large variability due to random grain boundary traps [1], an adequate modeling of the trap states in poly-Si is crucial to analyzing the device characteristics. There have been several works [1-4] engaging in modeling and simulating the effects of GBs in poly-Si channel in the past. However, a full 3D study reflecting the nature of arbitrary shape in grain patterns is still lacking. In this work, utilizing a novel 3D Voronoi method to consider the GB patterns more accurately, we investigate the GB-induced variability for stackable NAND flash.

II. Simulation Methodology
Fig. 1 shows a summary of schematics and simulation methodologies employed in this work. 1D-rectangular [3], 2D-Voronoi [4], and 3D-Voronoi GB patterns are all performed and compared. The device is designed as a junction-free BE-SONOS TFT [5]. Trap states are implemented as interface traps at GBs. A trap-concentrated GB may capture charges and form a potential barrier which impedes free carriers [6]. Other pertinent device parameters are listed in Table 1.

The flow chart for both 2D- and 3D-Voronoi approaches to simulate random GB induced variation is shown in Fig. 2. The input parameter is the average grain size (d). For a given grain size, we can obtain various GB patterns by placing grain seeds randomly. Fig. 3 illustrates how the 3D Voronoi patterns are generated.

III. Results and Discussion
Using our proposed 3D Voronoi method, Fig. 4 shows the I_{DS}-V_{GS} dispersion with 200 random samples and their V_{th} distribution. The V_{th} distributions from all three methods are compared in Fig. 5 for devices with H_{ch} = 30 nm. We can observe that there is an unusual spike near V_{th} ≈ 0.75 V for the 1D and 2D grain cases. This stems from the devices that have no GBs in their channels. On the other hand, the spike seems to disappear for the 3D grain case because most of these devices possess GBs in their channel regions and hence devices with the smallest V_{th} become rare.

In Fig. 6 we use two devices to illustrate how the shapes of GBs influence the channel conduction. Both of these two devices have only one GB in their channel, however, device α has GB perpendicular to the current flow while device β does not. We can find from Fig. 6(b) that, under the same gate bias, their potential barrier heights are fairly different. This gate-modulated potential barrier height impacts the subthreshold characteristics through gate-induced grain barrier lowering (GIGBL) [1] and results in the highly correlated V_{α} and SS as shown in Fig. 7. In other words, in addition to the number of GB, the shape of GB also affects the V_{th} variation. Compared with the 1D and 2D grains, the 3D grain has more freedom in varying the GB shapes, thus exhibits different V_{th} variability.

Fig. 8 shows the cumulative probability for V_{th} and SS for devices with various channel heights (H_{ch}). It can be seen that as H_{ch} shrinks, the distribution becomes wider. Fig. 9 compares the V_{th} variation with the scaling of H_{ch} for 1D, 2D and 3D methods. It can be seen that the 1D and 2D methods tend to underestimate the σ(V_{th}) for devices with scaled H_{ch}. It indicates that a full 3D GB pattern needs to be employed to accurately simulate the GB-induced variability.

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References
Table I Device parameters used in this work

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Fig. 1 Schematics for (a) 1D-rectangular [3], (b) 2D-Voronoi [4], and (c) 3D-Voronoi GBs (this work).

Fig. 2 Flow chart describing the 2D and 3D Voronoi methods for simulating poly-Si channels.

Fig. 3 Flow for constructing 3D-Voronoi pattern. (a) Randomly place grain seeds. (b) Connect every seed to its neighboring seeds (dash lines). (c) Draw perpendicular bisectors (grey planes). (d) Completed 3D Voronoi diagram.

Fig. 4 The dispersion of $I_{on}-V_{GS}$ curves and its $V_{th}$ distribution (inset).

Fig. 6 (a) Two devices with different GB patterns and (b) their conduction band energy profiles (along the dash line in (a)) at $V_{GS} = 0.05$ V and $V_{GS} = 1$ V. The inset shows the assumed U-shaped trap energy distribution in these GBs.

Fig. 8 Cumulative probability for (a) $V_{th}$ and (b) SS with various channel heights ($H_{ch}$).

Fig. 9 Comparison of the $V_{th}$ variability between different GB patterns with various $H_{ch}$.