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A New 28nm HKMG CMOS Logic OTP Cell

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ABSTRACT

A new compact 28nm high-K metal gate one-time programmable (OTP) cell is proposed. The OTP cell was fabricated by a pure 28nm HKMG CMOS process without extra process or masking step. The OTP cell operation is based on a permanent breakdown of high-K gate dielectric of 28nm HKMG n-MOSFET. The new OTP cell shows very low power and fast program performance with an ultra-small cell area of 0.0425μm^2. By optimizing the operation, the OTP can efficiently operate at very low program current of 50μA with short program time of 100μs and more than 10^{5}X On/Off read window. Furthermore, the high density OTP cell also has superior reliability characteristics in retention, disturb, and temperature read. Those all make the cell be a promising solution of logic NVM applications.

Introduction

Recently, logic embedded one-time programmable (OTP) memory has attracted much interest for growing demand on code, secure storage or customized settings. Different kinds of programming mechanism have been reported, including anti-fuse [1-7], fuse [8] and charge trapping [9-10] memory. Proposed by Shi (2011) [8], standard contact fuse uses high current pulse of 2.4mA with 3V to destroy the contact and different current level would indicate on/off state. However, by taking advantage of low program current, less power consumption and small cell size, the anti-fuse OTP is more suitable for low cost and energy conservation [1]. In this work, a new structure realized in 28nm high-k metal gate (HKMG) CMOS logic process without extra masks or process steps is firstly proposed. With a small cell size, low program current and ultra-fast program speed, this cell is a powerful candidate for OTP solution in advanced CMOS logic technologies.

Cell Structure and Characteristics

The TEM pictures of Fig. 1 illustrate the OTP cell structure and the breakdown region, which consists of two n-channel HKMG core transistor gates in series. One transistor is treated as a selector, while the other one as a storage node. Additionally, shown in high resolution TEM of Fig. 1 as well, the high-K gate dielectric is perfectly formed between N^+ diffusion and the metal gate for a fresh cell. After programmed, the gate dielectric is rapidly damaged and results in a low resistance path from metal gate to N^+ diffusion. On the other hand, as illustrated in Fig. 2, this cell can be further arranged in high density NOR-type array where source line (SL) is parallel to word line (WL) and orthogonal to bitline (BL). Table I summarizes the operation conditions of the new OTP memory cell. A selected cell can be fast programmed with V_{WL}=0.85V, V_{SL}=4.5V and V_{BL}=0V within 100μs while the unselected one can be inhibited with V_{BL}=floating. For reading, both WL and SL are biased at 0.85V and BL is connected to ground. Sensing current can be detected, and a large read current reveals an On-state whereas small current indicates an Off-state.

As demonstrated in Fig. 3 and Fig. 4, higher SL or WL voltage will speed up the programming procedure and ultra-fast programming speed (<50ns/cell) can be realized. However, in order to protect devices from high voltage stress, to avoid possible soft breakdown and to maintain fast enough speed, a pulse biased at V_{WL}=0.85V, V_{SL}=4.5V with 100μs width is utilized for array consideration. Furthermore, Fig.5 indicates the variation of program speed under different temperature. When heating the cell from 0℃ to 125℃, the program time of the cell accordingly decreases from 400μs to 7μs. Namely, higher temperature operation accelerating high-K gate dielectric breakdown is observed.

On the other hand, in spite of slightly different read current level of Off-state caused by cell-to-cell variation, excellent read disturb immunity under different temperature is clearly displayed in Fig. 6. In addition, Fig. 7 further demonstrates that ten-years lifetime is predicted when biased at V_{SL}=2.3V, which implies that the data storage for more than ten years can be ensured for this cell when the read condition of Table I is adopted. As presented in Fig. 8, there is no program disturb concern for unselected cell even up to 100k disturb cycles. Moreover, no significant change of both states after 1k hours bake at 150℃ are shown in Fig.9. Finally, Fig.10 summarizes the OTP cell cumulative distribution of current levels at On and Off states. Even considering cell-to-cell variation, more than 10^{5}X on/off read window is still guaranteed for array operation.

Conclusion

A new one-time programmable (OTP) non-volatile memory (NVM) cell, fully compatible to 28nm high-k metal gate (HKMG) CMOS logic process, is proposed. This cell with small cell size features low program current, fast program speed and large on/off ratio. Notable scalability and reliability are demonstrated as well. These superior characteristics make the new cell an outstanding choice of next generation OTP memory.

References

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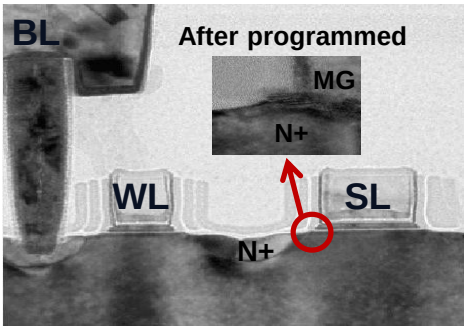

Fig. 1 TEM pictures of cross section and breakdown point of proposed 28nm 2T OTP memory cell

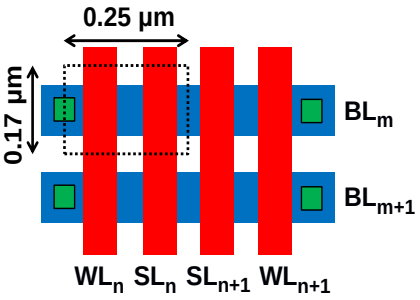

Fig. 2 2x2 NOR-type cell array layout where SL is applied high voltage when the cell is programmed

		WL	SL	BL	PW
Prog.	sel.	0.85	4.5	0	0
	unsel.	0	0	F	0
Read	sel.	0.85	0.85	0	0
	unsel.	0	0	F	0

Table I Operation conditions of 28nm CMOS logic OTP cell in a NOR array

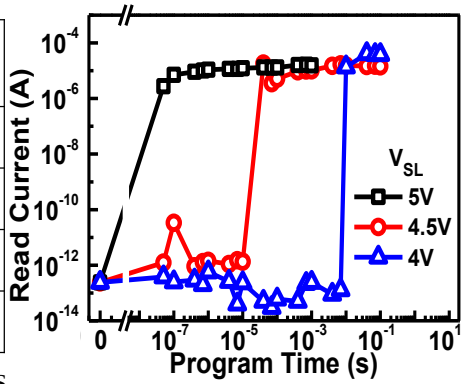

Fig. 3 Time to program characteristics at V_{WL}=0.85V with different SL voltages

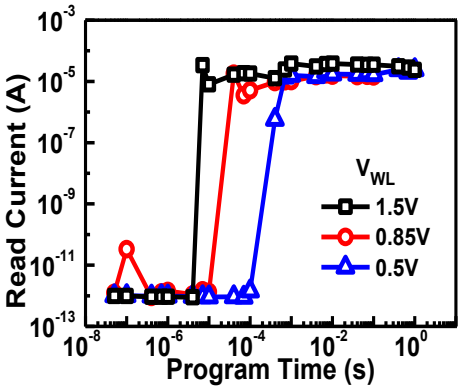

Fig. 4 Time to program characteristics at V_{SL}=4.5V with different WL voltages

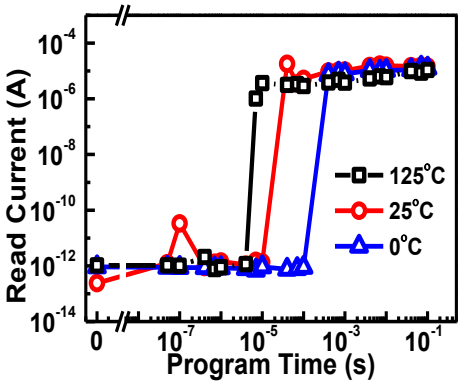

Fig. 5 Time to OTP program at V_{WL}=0.85V, V_{SL}=4.5V with different temperature

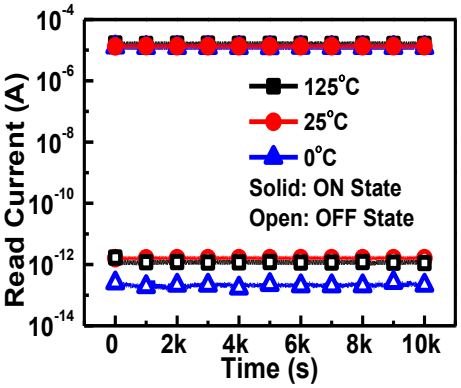

Fig. 6 10k seconds read DC stress under different temperature

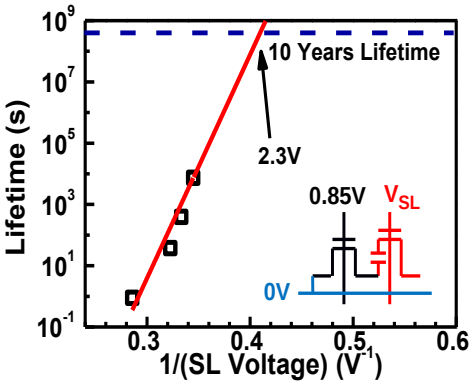

Fig. 7 Lifetime estimation and 10 years lifetime prediction for data storage

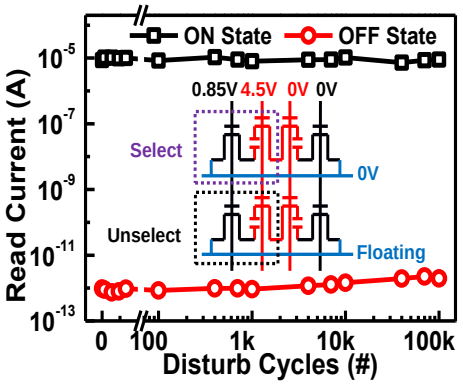

Fig. 8 Program disturb for the unselected cell operated at V_{WL}=0.85V, V_{SL}=4.5V for 100μs where V_{BL}=floating

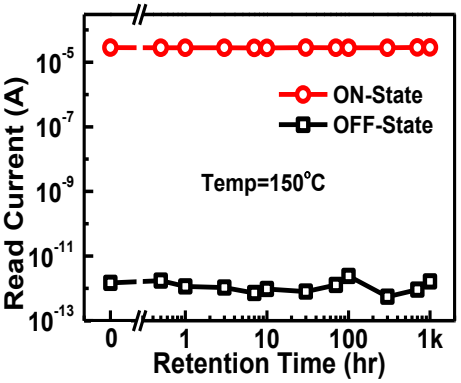

Fig. 9 Data retention test at 150℃ for 1k hours

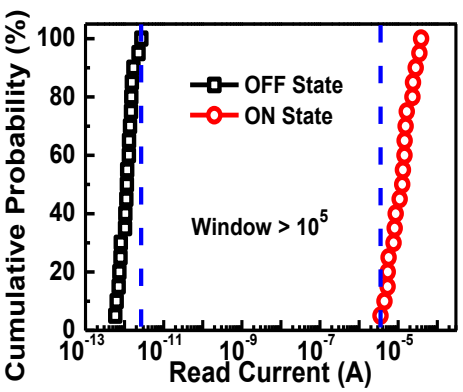

Fig. 10 Cumulative distributions of current levels of on/off states