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Improvement of Cycling Disturbance and Yield Enhancement of ReRAM using Susceptibility-Aware Write

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1. Introduction

Resistive RAM (ReRAM) is a promising candidate for next generation non-volatile memory due to low switching current, high scalability, simple structure and, high speed switching operation [1]. To control large resistance variations, ReRAM employs incremental step pulse programming (ISPP) of which each step comprises of a programming-verify process. The conventional ISPP (c-ISPP), however, consumes large power and takes long time because the number of incremental steps must be large enough to cover wide distribution of susceptibility of the worst cells [2]. The adaptive control of the step size in ISPP (a-ISPP) was proved that the power dissipation is reduced by 50% with a 2.25 times faster write speed [3]. While investigating a-ISPP we found that the reliability of ReRAM is sensitive to the types of ISPPs.

This paper addresses the improvement of reliability of ReRAM, such as immunity to cycling disturbance, and consequent yield enhancement by careful design of ISPP waveforms. The logic chip is fabricated using a 350-nm technology and integrated with 1-Kb HfO_x array chip.

2. Cycling Disturbance Analysis with Adaptive ISPP

Fig. 1(a) shows measured and modeled I-V curves of a HfO_x bipolar ReRAM cell. ReRAM utilizes the change of resistance value to store data where the resistance value is switched between low (LRS or set) and high resistance states (HRS or reset) by applying a voltage pulse or a current pulse across cell. To set the ReRAM cell, positive bias is applied on top electrode, and negative bias for reset. The modeled I-V curve agrees well with the measured one because the model includes transition of set/reset current, degradation due to aging or disturbance, and variation of ReRAM cell [4]. Fig. 1 (b) shows measured and modeled curves of c-ISPP with a worst cell. In the c-ISPP, many incremental steps are needed to store data in a worst cell. Fig. 2 describes the concept of a-ISPP. In our work, the current mode flash ADC is used as a bit line sense-amplifier [3]. Therefore, the current of ReRAM cell is converted into 4-bit digital codes during read or verify operation where MSB represents the data of ReRAM cell and remaining LSBs show the variation of cell current. In a-ISPP, the states of ReRAM cells are divided into 3 groups after initial stressing during reset, and then the size of second stress is adjusted based on the states. Fig. 3 illustrates the comparison of stressing pulse trains for c-ISPP and a-ISPP. In c-ISPP, BL voltage is fixed at "Vwr/2" and initial WL voltage is "-Vwr/2" in reset case, then the WL voltage is decreased by fixed amount. The large number of steps is required for worst cell group (state3) in c-ISPP. In the a-ISPP, however, a small number of pulse steps are enough for all groups of cells because the harder the cell is, the stronger the second stress is. Fig. 4 shows the comparison of simulation results with c-ISPP and a-ISPP. The a-ISPP effectively reduces the number of steps that is also proved by the measured data [3]. Fig. 5 plots the number of effective cycling with c-ISPP and a-ISPP. The effective cycling stands for the number of activating WL and BL with respect to that of external write command. In this study, eight cyclic stresses are asserted on ReRAM cells on the same row per one command of c-ISPP, while four cycles for a-ISPP. The number of effective cycling with a-ISPP is reduced by 50 % as compared with c-ISPP. The cycling disturbance of ReRAM cell is critical issue when adjacent cells are repeatedly over-written because the initial resistance value is changed with increasing cycles [5]. Fig. 6 shows measured results of cycling disturbance with c-ISPP and a-ISPP. The cycling disturbance of a-ISPP is improved by 40% with a normal cell and 54% with a weak cell at the read fail point. Fig. 7 describes statistical analysis of cycling disturbance with c-ISPP and a-ISPP. The measured data are statistically expanded to analysis the variability. We focus on the behavior of tail bits because initial sensing fail bit is generated by tail bits. The number of fail bit is 0.1% with c-ISPP, but the fail bit is not detected with a-ISPP after 10^5 program accesses.

3. Yield Enhancement with Improved Write

Fig. 8 shows a concept of yield enhancement with improved write. In conventional memory test, cells are tested with various conditions and the output results are just the information of "pass" or "fail". In our scheme, the state of cells is estimated by ADC. Therefore, we can define a soft fail cell which is in the boundary between pass and fail. For example, the "0100" state can be defined as the soft fail cell. The "address comparator" in Fig. 8 registers specific address of fail cells during test mode. The "match" signal goes to high when address matches with registered one and then the BL voltage is boosted by pre-determined amount as shown in Fig. 9. Consequently, the soft weak cells are stressed with more strong pulses. Bias and timing conditions of a proposed scheme are schematically illustrated in Fig. 9. The soft weak cell is successfully sensed with a proposed scheme. Fig. 10 compares the measured yield results of set/reset states with a proposed write scheme. The yield is improved from 97 % to 100 %. We simulated the program operation with a soft fail cell to monitor a behavior of reset current with a proposed write scheme as shown in Fig. 11. Although the switching property is improved with increased BL voltage, the BL boosting voltage is carefully optimized during test mode to avoid unexpected disturbance.

4. Conclusions

We evaluated cycling disturbance of adaptive step-size control of ISPP using both simulation and measurement. The cycling disturbance is improved by 54% and the ReRAM cell is successfully sensed after 10^5 program accesses with the a-ISPP. We also proposed a improved write scheme that boosts the BL voltage of soft fail cells, which results in yield enhancement from 97 % to 100 %.

Acknowledgement

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Reference

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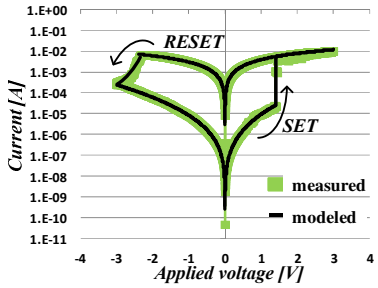
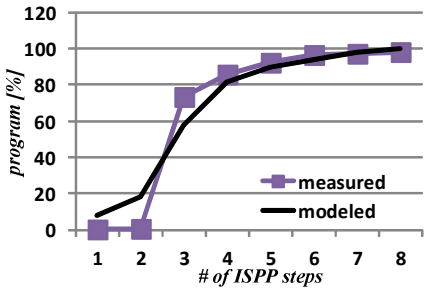


(a)



(b)

Fig. 1 Measured and modeled I-V (a) and conventional ISPP (b) curves of a HfO_x ReRAM cell.

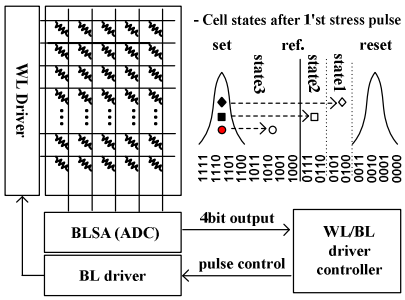


Fig. 2 Concept of adaptive ISPP. ReRAM cells are divided into 3 states after initial stressing during reset.

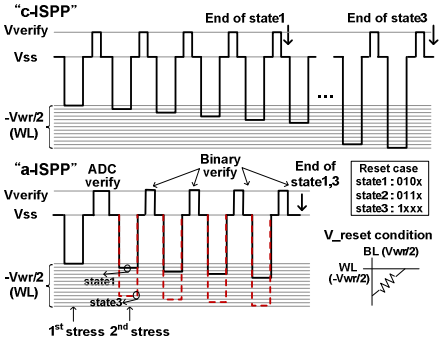


Fig. 3 Stressing pulse trains for c-ISPP and a-ISPP.

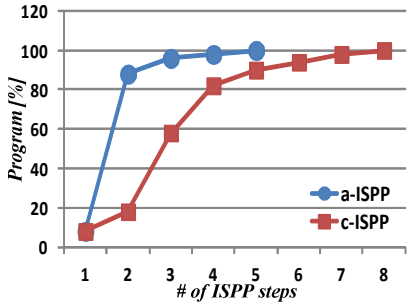


Fig. 4 Comparison of simulation results with c-ISPP and a-ISPP.

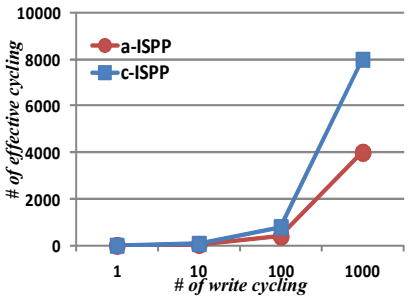


Fig. 5 Number of effective cycling with c-ISPP and a-ISPP.

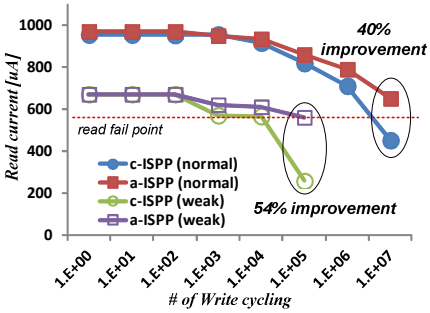


Fig. 6 Measured results of cycling disturbance with c-ISPP and a-ISPP.

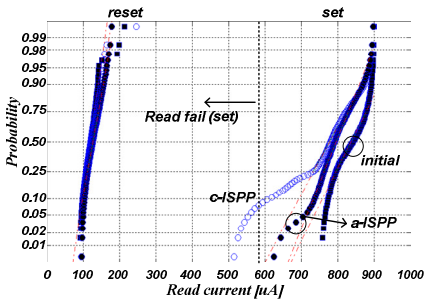


Fig. 7 Statistical analysis of cycling disturbance with c-ISPP and a-ISPP after 10^5 program accesses.

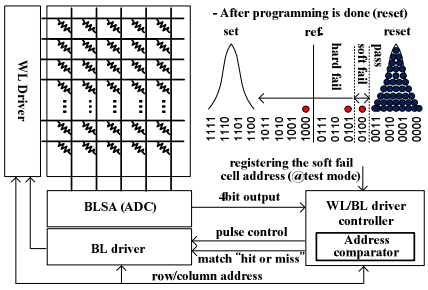


Fig. 8 Concept of yield enhancement with a improved write scheme.

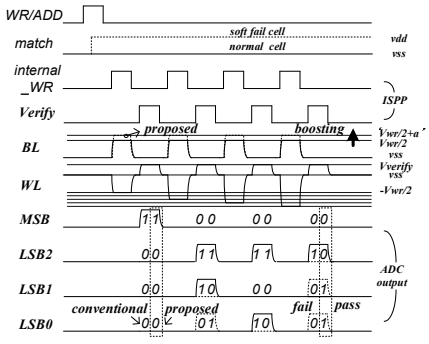


Fig. 9 Bias and timing conditions of a proposed write scheme. BL voltage is boosted with soft fail cells.

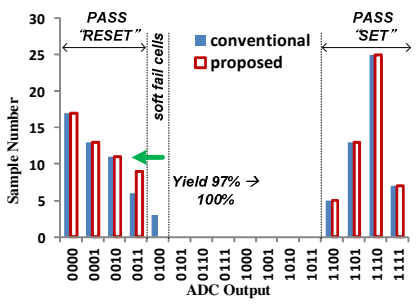


Fig. 10 Measured yield results of set/reset states with a proposed write scheme.

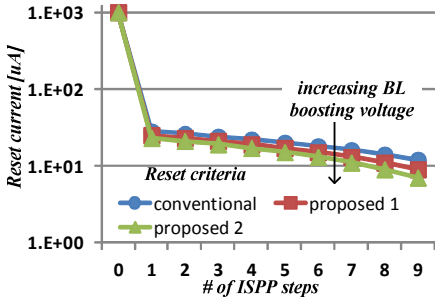


Fig. 11 Reset simulation of a soft fail cell with the proposed scheme. The BL boosting voltage is optimized during test mode.