

Mb-Class Array Level Investigation of Program Verify Methods for Al_xO_y ReRAM

Sheyang Ning^{1,2}, Tomoko Ogura Iwasaki¹ and Ken Takeuchi¹

¹ Chuo University, Tokyo, Japan, ² University of Tokyo, Tokyo, Japan

E-mail: ning@takeuchi-lab.org

Abstract

Various set and reset program methods are investigated on a 50nm, Mbit-class ReRAM chip, and program bit error rates (BERs) are compared in 4×4 matrices. Further, an optimized reset method is proposed, which decreases reset time by over one order of magnitude and improves both reset and set bit error rate.

1. Introduction

Resistive random access memory (ReRAM) is considered a promising next generation non-volatile memory [1]. The previous research on single HfO_2 ReRAM devices has found that the program verify method has a large effect on device endurance [2]. In [3], the combinations of three types of reset pulse width modulations and three types of set voltage modulations are applied on endurance testing of discrete 50nm Al_xO_y ReRAM devices. However, these methods have been developed for single device program. When data is programmed in pages, the concepts require adaptation and statistical confirmation. In this work, a methodology for array level verification is introduced and a comprehensive investigation of program methods is conducted on a Mbit-class Al_xO_y ReRAM array. Both voltage and pulse width modulation methods are investigated for reset and set w/ verify. The reset, set and total BERs are compared in 4×4 matrices, after 2000 endurance cycles. In addition, a new method is proposed to optimize the reset pulse width increment, which simultaneously decreases the reset time by over one order and improves reset and set BERs. These results support the conclusion in [3], in that reducing reset pulse width also suppresses over-reset resulting in the improved endurance.

2. Measurement Results and Discussions

Investigation of program verify methods

A description of the Mbit-class, 50nm one-transistor one-resistor (1T1R) Al_xO_y ReRAM test chip and device structure is given in Fig. 1. Set program decreases the device resistance to the low resistance state (LRS) in which $R \leq 108\text{k}\Omega$. The basic set pulse is a 1.8V, 100ns pulse applied to the bit line (BL) with 0V on the source line (SL). Reset program increases the device resistance to the high resistance state (HRS) in which $R \geq 505\text{k}\Omega$. The basic reset pulse is opposite polarity, with BL=0V and SL=1.5V, for 20ns. The flow for endurance test is in Fig. 2. Forming and 1000 set-reset aging cycles are first applied to condition the ReRAM array. Then 2000 reset w/ verify plus set w/ verify cycles are evaluated. A reset w/ verify can take up to 20 tries until $\text{BER} < 1\%$. The stress level of these 20 pulses steps up from the initial pulse stress, and is only applied to the reset failed bits. The stress of the initial pulse can be modified after one endurance cycle. In Fig. 3, the pulse width modulation methods W1, W2 and voltage modulation methods V1, V2 are explained. For reset as an example, both W1 and W2 increase reset pulse width in 40ns steps, up to 20 tries, whereas V1 and V2 increase reset voltage in 0.1V steps. W1 and V1 have a constant initial pulse width and voltage, respectively. On the other hand, in W2 and V2, the initial pulse width or voltage is increased 40 ns if reset BER after the previous reset program is larger than 1%. If BER is less than 1%, the initial value is kept because the stress level is judged sufficient. W2 provides stronger program stress than W1, due to the incrementing of the initial stress. V1 and V2 are similar but the reset voltage is increased by 0.1V, rather than pulse width. Set w/ verify is similar to the reset w/ verify in Fig. 2 and Fig. 3, with opposite polarity. The array resistance distributions before and after forming are shown in Fig. 4. Fig. 5 shows example of bit errors that are counted in the BER. It can be seen that in this array-based scheme,

bit that fail to program within the 20 tries can continue to be re-used for soft error, because it can successfully be programmed in later cycles. Hard failure on the other hand, is not recoverable. In this work, BER is caused by both soft errors and hard failure errors.

Figure 6 compares reset, set and total BERs on 4×4 matrices, after 2000 endurance cycles for each condition. The lowest total BER is provided by the W2-reset, V1-set method. In Fig. 7, by using the V1-reset, V1-set method, due to the high reset voltage from 1.5V to 3.4V in 20 tries, significant LRS bits are observed as early as the 10th endurance cycle. This explains the large BER for V1- and V2-reset methods in Fig. 6(a). In Fig. 8, by applying W2 method on set, even though set pulse width was increased over 80μs at the 2000th endurance cycle, set could not be successfully completed. Therefore, W1 and W2 methods cause large set BER, as in Fig. 6(b). In Fig. 9(a), by using the W1-reset, V1-set method, the cumulative resistance distribution is compared when the endurance cycle at 100, 1000 and 2000. The LRS resistance is stable with endurance cycling whereas HRS resistance is largely degraded [4], which accelerates the increase of the reset BER. In Fig. 9(b), reset BER is reduced due to the initial reset pulse width increment in W2 method (Fig. 11) which provides stronger reset strength when HRS degrades.

In [2], the set voltage increment is needed to extend endurance of HfO_2 ReRAM device [2]. This difference can attribute to material characteristics. The HfO_2 ReRAM device becomes hard-to-set with device cycling [4, 5].

Over-reset reduction and discussion

An optimized reset pulse width modulation method, $W_{\text{optimized}}$, is proposed with the algorithm given in Fig. 10. The pulse width step up is accelerated during the 20 tries of reset w/ verify which provides sufficient reset strength to program hard-to-reset devices (Fig. 10(a)). In Fig. 10(b), the initial reset pulse width can be decreased as well as increased to maintain a certain BER first level, arbitrarily given here as 50%. Comparing the $W_{\text{optimized}}$ -reset method with W2-reset method, over one order of reset pulse width reduction is obtained in Fig. 11.

Fig. 12 shows the set and reset BERs for W2- and $W_{\text{optimized}}$ -reset methods. In Fig. 12, V1 method is used for set verify. Both reset and set BER are reduced when endurance test is extended to 4000 cycles. The trend of the reset BER for the W2-reset method appears to increase at a faster rate than for the $W_{\text{optimized}}$ -reset method. Although hard failures and soft errors are both included in the BER, the increasing trend of BER suggests that the large reset pulse width by W2-reset method causes over-reset or premature wear-out of the ReRAM devices and fast increase of the reset BER.

3. Conclusions

To decrease Al_xO_y ReRAM program BER in M-bit class arrays, comprehensive analysis with various program-verify methods for array-level implementation has been done in this work. Furthermore, an optimized reset method is also proposed, which simultaneously reduces reset pulse width, reset BER and set BER.

Acknowledgements

The authors would like to express thanks to K. Miyaji, K. Johguchi, C. Sun, N. Awaya, H. Akinaga for their contributions to this paper.

References

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Test chip:	
Size	Mbit-class
Technology	50nm
Memory device	1T1R Al_xO_y
Memory tester	Advantest T5781

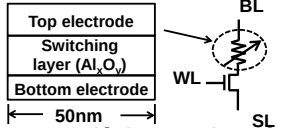


Fig. 1. Al_xO_y ReRAM device structure and measurement equipment for the test chip.

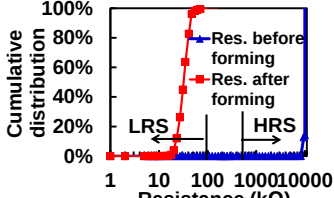


Fig. 4. Resistance cumulative distribution before and after forming.

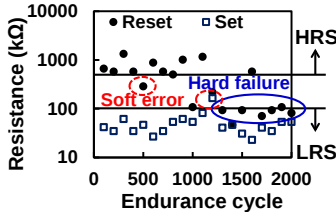


Fig. 5. Resistance vs. cycling of one bit in array. Soft errors are recoverable with subsequent cycling. Hard failures correspond to device break-down.

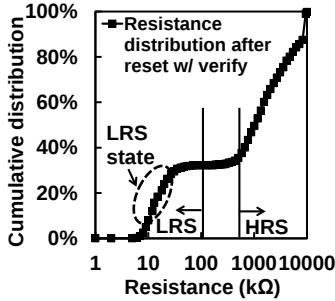


Fig. 7. Resistance distribution for V1-reset and V1-set method after 10th endurance cycle. The large number of LRS bits occurs due to high reset voltage.

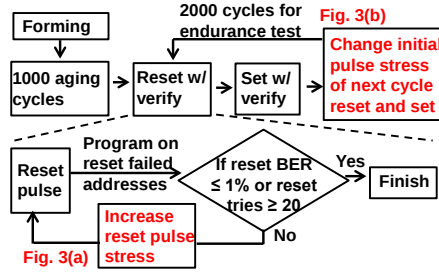


Fig. 2. Endurance test flow. Reset increases page resistance to $R \geq 505\text{k}\Omega$. Reset w/ verify completes if reset bit error rate (BER) $< 1\%$ or reset tries reaches 20. Similarly, set w/ verify decreases resistance to $R \leq 108\text{k}\Omega$.

V_{init} : Initial pulse voltage T_{init} : Initial pulse width			
	V1	V2	W2
Initial pulse for each verify cycle	Fixed	Keep the V_{init} (if $\text{BER} \leq 1\%$), $V_{\text{init}} + 0.1\text{V}$ (if $\text{BER} > 1\%$)	Fixed
Pulse modulation during verify	V_{init} $V_{\text{init}} + 0.1\text{V}$ $V_{\text{init}} + (m-1) \times 0.1\text{V}$	T_{init} $T_{\text{init}} + 40\text{ns}$ $T_{\text{init}} + (m-1) \times 40\text{ns}$	

Fig. 3. Methods to modulate initial reset stress during reset w/ verify. (b) change stress initial setting for next endurance cycle program.

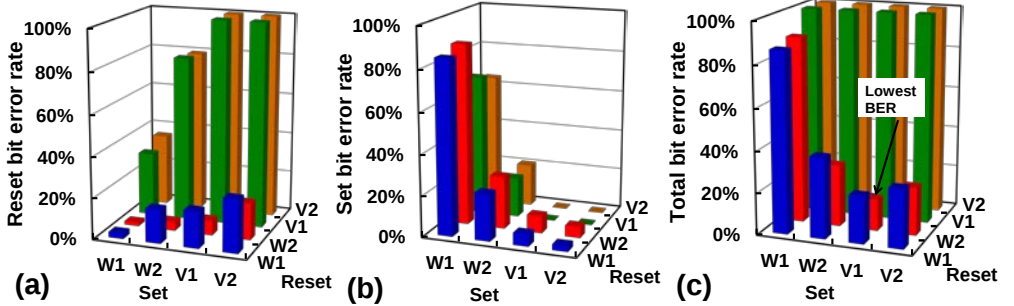


Fig. 6. Bit-error-rate (BER) in 4×4 matrices. (a) Reset BER which is measured after reset: Voltage increase methods V1 and V2 increase reset-BER. (b) Set BER measured after set: Pulse width increase methods W1 and W2 also increase set BER. (c) W2-reset and V1-set method shows the lowest total BER.

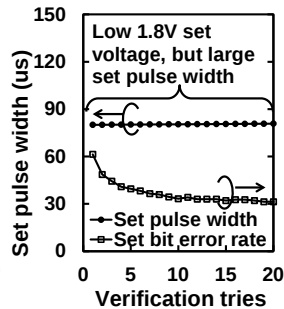


Fig. 8. Set BER and set pulse width for W1-reset, W2-set case. Even large pulse widths cannot effectively set.

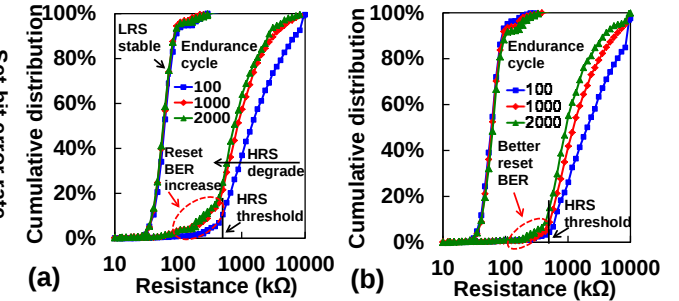


Fig. 9. Resistance distribution during cycling of (a) W1-reset V1-set method, (b) W2-reset, V1-set method. In (a), reset BER is increased due to HRS degradation. In (b), reset BER is lower when initial reset pulse width is incremented by W2 method.

BER_{first}: bit error rate after first reset pulse
 $T_{\text{init}}(L)$: initial reset pulse width at cycle L

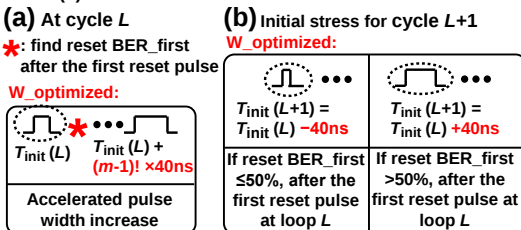


Fig. 10. Optimized reset pulse width modulation method, $W_{\text{optimized}}$. (a) The increment step for the pulse width during reset verify is accelerated by a factorial function. BER_{first} is reset bit error rate after first reset pulse at cycle L . (b) The proposed $W_{\text{optimized}}$ method provides decrease or increase options to the initial reset pulse width based on the reset BER in the previous reset verify.

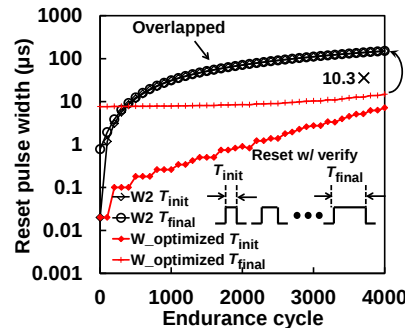


Fig. 11. Comparison of pulse widths for the initial (T_{init}) and final (T_{final}) pulses. The conventional W2-reset and the proposed $W_{\text{optimized}}$ methods are compared. In W2-reset case, T_{init} and T_{final} are almost the same. With $W_{\text{optimized}}$ -reset, over one order of reset pulse width reduction can be achieved at the 4000th endurance cycle.

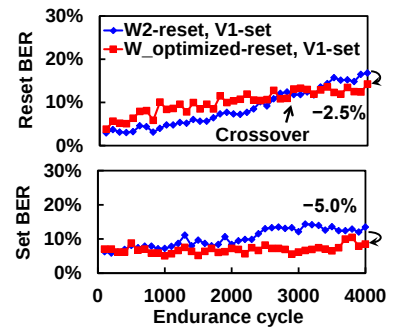


Fig. 12. BER comparison result between W2- and $W_{\text{optimized}}$ -reset methods. The set method for both is V1. Since in W2-reset the pulse width is rapidly increased, high stress is applied to the device, which causes the fast increase of reset BER due to device over-reset.