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A Novel Self-rectifying WSi_xO_y Device in a Double-density Architecture for 3D ReRAM

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Abstract

3D stacked ReRAM is difficult to realize because of the difficulties in bipolar selecting device and the lack of suitable architecture to decode the 2-terminal device for 3D array. In this study, we report a novel self-rectifying WSi_xO_y ReRAM with good high temperature data retention and read disturb immunity. Rapid thermal oxidation (RTO) of WSi_x forms the WSi_xO_y layer as both the storage node and a rectifying device with the p+ poly electrode. The simple process to achieve this self-rectifying device allows us to incorporate it into a double-density 3D architecture that adopts a regular MOSFET for X-Y decoding. We estimate this device and architecture that can easily provide operation margins for up to 16 layers of 3D ReRAM.

I. Introduction

Resistive memories attract much attention due to its simple MIM (Metal-Insulator-Metal) structure and promising scalability [1]. However, since NAND Flash can stack up vertically with many layers 2D ReRAM has little advantage in cost [2]. 3D stacking of ReRAM turns out very challenging since (1) the lack of good bipolar selecting device, and (2) the difficulty of decoding a 3D array of 2-terminal devices. In this work, we report a novel self-rectifying device that can be easily embedded in a 3D architecture using a regular MOSFET at the bottom of the vertical string for X-Y decoding [3, 4]. Furthermore, our proposed new device/structure is not only simple and readily made with familiar CMOS materials and process but also provide 2-bits/cell density without MLC.

II. Novel Self-rectifying p+ Poly/WSi_xO_y Cell

Figure 1 shows the schematic process flow of a self-aligned WSi_xO_y ReRAM with a p+ poly electrode. The WSi_x under the contact hole is oxidized by low temperature 350°C rapid thermal oxidation (RTO). An EDX image of such a device is shown in **Fig. 2**. **Figure 3** shows the I-V curves and band diagrams for p+ poly/WSi_xO_y and n+ poly/WSi_xO_y respectively. Asymmetrical I-V characteristics are observed for both n+ poly and p+ poly electrodes and may be explained by simple metal-insulator-semiconductor (MIS) phenomena. However, only the p+ poly/WSi_xO_y cell maintains the asymmetric I-V property after the forming process as shown in **Fig. 4**. The forward current is used to set and reset the p+ poly/WSi_xO_y cell and examine the cycling property.

Figure 5 shows the read I-V curves of the p+ poly/WSi_xO_y cell after pulse cycling test for both SET and RESET states. The SET/RESET state can be distinguished in the forward current mode but is indistinguishable in the reverse current mode, because the resistance of the reverse bias dominates. This is exactly the behavior expected of a self-rectifying cell.

J-V curves at various temperatures of the p+ poly/WSi_xO_y cell were measured to validate the conduction mechanism. As shown in **Fig. 6**, the ln (J/T^2) vs. $1/k_BT$ behaviors are typical for barrier lowering by the electric field in thermionic emission for both the RESET and the SET states. The barrier heights for both the RESET and SET states are similar, ~0.25eV. This suggests that the barrier only provides the rectifying function, but the HRS and LRS still come from oxygen vacancies that are electrochemical in nature, as in most TMO ReRAM.

Figure 7 shows the thermal stability test of the p+ poly/WSi_xO_y cell. A 10X resistance window is well maintained after 150°C baking.

III. Proposed 3D p+ Poly/WSi_xO_y ReRAM Structure

Figure 8 shows the proposed 3D p+ poly/WSi_xO_y ReRAM structure [4]. In this new architecture the WSi_xO_y device is in horizontal direction, and a device is formed on each side of the poly pillar, resulting in two devices per unit cell area. The WSi_x layers are patterned by lithography/etching and serve as both the memory elements (the oxidized ends) and the interconnect (since except in the small open areas the rest of the WSi_x is not oxidized) to memory cells. The pillar electrode is formed by p+ poly that is connected to the drain side of an access transistor, which controls and isolates 2N ReRAM elements in the N-layer structure. Since the p+ poly/WSi_xO_y cell is self-rectifying no other selecting device is needed for the cells on the same pillar. **Figure 9** shows a TEM picture for a 2-layer WSi_xO_y-stacked device. It shows good uniformity of the sidewall WSi_xO_y film for both top layer and bottom layer, and its thickness is about 40A. **Figure 10** shows the corresponding EDX analysis, which approximately confirms the TEM observation.

IV. Read Margin Evaluation for 3D ReRAM

Even though the X-Y decoding is done by a MOSFET there are still other leakage paths within each Z plane, and between planes. These need to be isolated by the self-rectifying device. **Figure 11** illustrates the proposed 1/3 V_{read} scheme for a simple 2*2*3 array [5]. The selected pillar electrode is applied V_{read} and the unselected pillar electrodes are floating. The selected Z layer is grounded and 1/3 V_{read} is applied to all unselected Z layers. Thus all unselected devices in the unselected pillar are reverse biased, and only the selected device is forward biased. This allows the reading of the resistance state of the selected device.

Figure 12 illustrates the sneak leakage paths and how the read margin is calculated. Each sneak path goes through two types of memory cells, one reverse biased and one forward biased. The reverse biased cell blocks the leakage current. In the worst case, all adjacent cells are at LRS and the DUT is at HRS, and the read margins are conservatively estimated using the worst-case scenario. **Figures 13** shows the calculated read margins with fixed resistance window of 10X for various numbers of 3D layers. As shown in **Fig. 14**, the read disturb test using various read voltages (+0.6 and -0.2 V for 1,000s) reveals that both RESET and SET states are immune to read disturbance. The self-rectification, SR = $R_{LRSreverse}/R_{LRSforward}$, is a critical parameter that determines the effectiveness of blocking the sneak leakage paths. With SR = 10^5, 16 layers is possible for a memory block of 1Mb as shown in **Fig. 15**.

V. Conclusion

A novel self-rectifying p+ poly/WSi_xO_y ReRAM device having excellent performances such as good data retention and read disturb immunity is successfully demonstrated. Further, the read margins for various conditions in the 3D array are estimated.

References:

[1] B.Govoreanu et al., *IEDM Tech. Dig.*, pp. 729-732, 2011.
[2] Akira Goda et al., *IEDM Tech. Dig.*, pp. 13-16, 2012.
[3] I. G. Baek et al., *IEDM Tech. Dig.*, pp. 737-740, 2011.
[4] W.C. Chien et al., *VLSI Tech. Symp.*, pp. 153-154, 2012.
[5] A.Chen, *Trans. Electron Devices*, vol. 60 pp. 1318-1326, 2013.

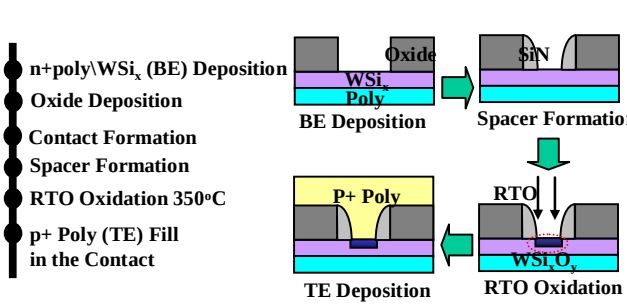

Fig.1 Key process flow for p+ Poly/WSi$_x$O$_y$ ReRAM device. The memory area is self aligned after contact hole formation. 350°C RTO is used to convert the WSi$_x$ into WSi$_x$O$_y$. Finally, p+ Poly is deposited above the WSi$_x$O$_y$ as the top electrode.

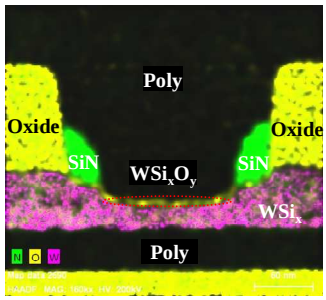

Fig.2 EDX mapping for the self rectifying poly/WSi$_x$O$_y$ cell. The WSi$_x$O$_y$ is also formed by 350°C RTO and is about 40Å. Then the poly film is deposited as the top electrode .

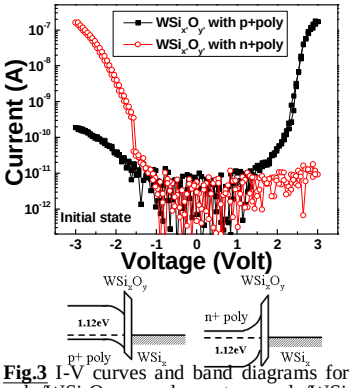

Fig.3 I-V curves and band diagrams for p+ poly/WSi$_x$O$_y$ and n+ poly/WSi$_x$O$_y$, respectively. Negative voltage is forward bias for n+ poly, and reverse bias for p+ poly.

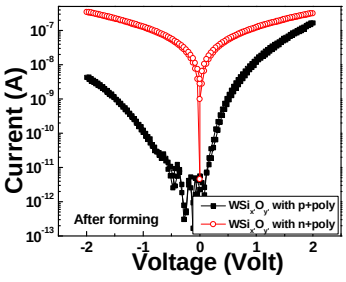

Fig.4 After forward forming voltage (negative for n+ poly /WSi$_x$O$_y$ and positive for p+ poly/WSi$_x$O$_y$), symmetric I-V is obtained for n+ poly/WSi$_x$O$_y$, but asymmetric I-V is obtained for p+ poly/WSi$_x$O$_y$.

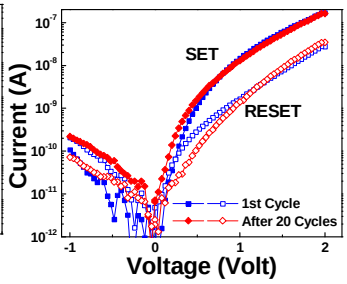

Fig.5 Read I-V curves for RESET and SET. The self-rectifying property is well preserved after cycling. Both RESET and SET show low leakage current under reverse bias.

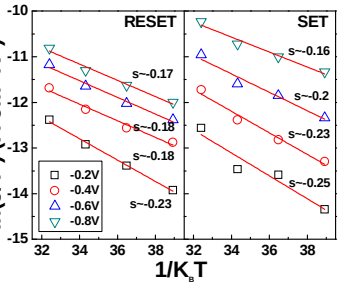

Fig.6 ln(J/T²) versus 1/k$_B$T curves for the RESET and the SET states at various biasing voltages. The behaviors are well predicted by thermionic emission.

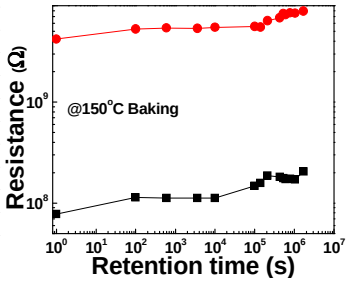

Fig.7 Retention test at 150°C of the self-rectifying p+ poly/WSi$_x$O$_y$ ReRAM cell. The resistance window is well maintained after 470 hours of baking.

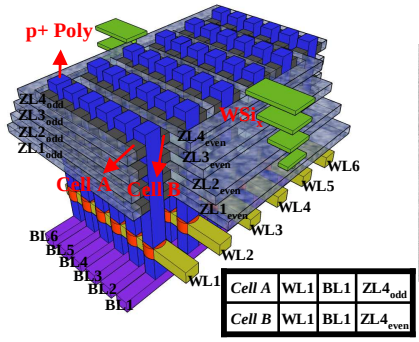

Fig.8 Proposed 3D structure for WSi$_x$O$_y$ based ReRAM and operation table. The pillar electrode is p+ poly while the sidewall ReRAM is WSi$_x$O$_y$. WL and BL are used to select the transistor which defines the X-Y coordinate of the pillar electrode. ZL is used to define Z coordinate. Each cell contains two devices.

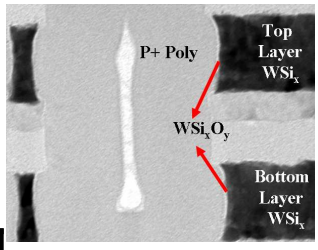

Fig.9 TEM picture for the 2-layer sidewall WSi$_x$O$_y$ device.

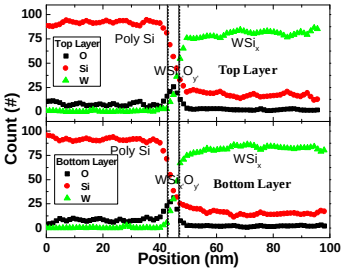

Fig.10 EDX analysis for the 2-layer WSi$_x$O$_y$ device. The thickness of oxidation for both bottom and top layers is 40Å.

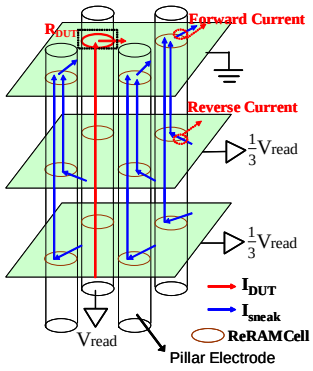

Fig.11 The schematic of the read operation for a (2*2*3) 3D array The possible sneak leakage paths during read operation are shown.

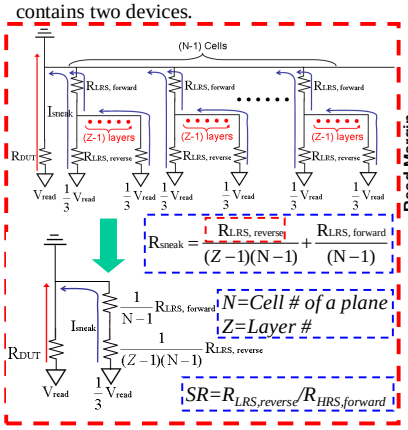

Fig.12 Worst-case read margin. The adjacent cells near the selected cell are all in LRS.

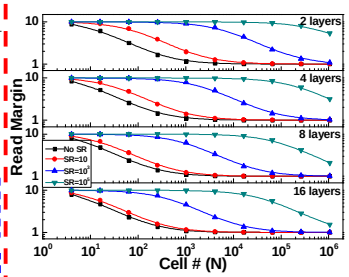

Fig.13 Read margin calculation with fixed resistance window of 10X (HRS/LRS) for various vertical layers. The self-rectification (SR) is a critical parameter that determines the feasible array size.

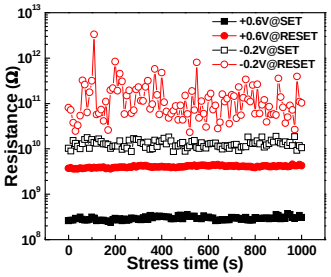

Fig.14 Read disturbance test. Both RESET and SET states show negligible read disturbance under both read voltages for 1,000s.

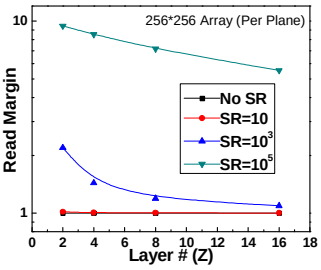

Fig.15 Read margin calculation for a 256*256 tile per plane for various layer numbers. SR = 10^5 is needed for 1Mb tile size.