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Excellent Reliability and Switching Uniformity of RRAM by Optimizing SET/RESET Pulse Shape to Minimize Current Overshoot

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1. Introduction

Recently, resistive random access memory (RRAM) has been intensively studied as a promising cadidate for next-generation non-volatile memory application due to its excellent properties such as low power consumption, fast switching speed and high-density integration [1]. For pratical application of RRAM, pulse operation is necessary. In pulse operation, the influence of capacitance elements should be considered. Thus, it is also inevitble in RRAM operation because of its capacitor like Metal-Insulator-Metal (MIM) structure. Therefore deep understading on the effects of capacitance elements on pulse operation of RRAM is highly demanded. However, previous studies reported only the influence of extrinsic capacitance of RRAM [2].

In this study, we investigated the effects of both intrinsic and extrinsic capacitance elements, especially on reliability of RRAM. Based on experimental results, the optimized SET/RESET pulse shape was proposed and experimentally verified to significantly improve the variability and endurance in a typical RRAM device with W/Zr/HfO_2/TiN structure.

2. Experiments

Fig. 1 shows the fabrication process flow and schematic structure of RRAM. The 5nm-thick HfO_2 layer was deposited on a TiN substrate by atomic layer deposition system. To form oxygen vacancies, thermal annealing was performed under NH_3 at 700 ^{O}C. Then, Zr top electrode and W capping layer were deposited by sputtering system. Electrical measurements were performed using semiconductor device parameter analyzer.

3. Results & Discussion

Fig. 2 shows typical bipolar resistive switching behavior of the W/Zr/HfO_2/TiN device. After forming process, repeated switching behaviors were observed. The transient response during SET process directly showed the effects of capacitance elements on RRAM pulse operation (Fig. 3). Overshoot current resulting from capacitance elements was observed during the rising time of SET pulse. It is already reported that the overshoot current in SET process has severe effects on variability of low resistance state (LRS) [3, 4]. The transient response during RESET process also directly showed the effects of capacitance elements (Fig. 4). Noticeable overshoot current of 800uA with 200ns width was observed during the falling time of RESET pulse. This high overshoot current can change the state of RRAM cell from high resistance state (HRS) to LRS when repeatedly applied. Thus, it can cause HRS failure and bring severe effects in endurance (Fig. 5). Indeed, 10^3~10^4 cycles of equivalent pulse (inset of Fig. 6) applied to HRS RRAM cell caused state change to LRS, which means that the overshoot current observed in RESET process can also cause HRS failure (Fig. 6). Therefore, suppressing overshoot current in SET/RESET process as low as possible will improve the variability and endurance of RRAM device in its operation.

To investigate the origin of the effects of capacitance elements, equivalent circuit model was proposed for LRS/HRS including both intrinsic and extrinsic capacitance elements (Fig. 7). In LRS, filament region of RRAM can be described by resistance of LRS (R_{LRS}) and the other oxide region can be modeled by oxide capacitance (C_O) parallel-connected with high resistance (R_H). Also, extrinsic capacitance can be simplified by parasitic capacitance (C_P). In HRS, dissolved filament region can be modeled by capacitance (C_1) parallel-connected with resistance (R_1) and remaining filament region can be represented by resistance (R_2). The other regions can be described as the same as in LRS. According to this model, total capacitance in LRS ($C_{total,LRS}$) equals $Co+C_P$ while total capacitance in HRS ($C_{total,HRS}$) equals $C_O+C_P+C_1$. Therefore, overshoot current of HRS is larger than that of LRS since $C_{total,HRS}$ is larger than $C_{total,LRS}$. Consequently, suppressing overshoot current of HRS is more effective than suppressing that of LRS in order to improve the reliability of RRAM.

The effects of suppressing overshoot current at LRS/HRS were confirmed experimentally by comparing with the results of a conventional rectangular pulse. Since the overshoot current is due to capacitor current (I_C), it was successfully suppressed by increasing rising/falling time (dt), according to $I_C=C\times dVc/dt$. As expected, increase in falling time of SET pulse (Fig. 8 B) or rising time of RESET pulse (Fig. 8 C) did not make any noticeable improvement in reliability (Fig. 9 & 10), because both are corresponding to $C_{total,LRS}$ which is very small. On the contrary, increase in either rising time of SET pulse (Fig. 8 A) or falling time of RESET pulse (Fig. 8 D) successfully suppressed the overshoot current (Fig. 11 & 12), because both are corresponding to large $C_{total,HRS}$. Therefore, both rising time of SET pulse and falling time of RESET pulse were simultaneously increased to reduce the overshoot current resulting from $C_{total,HRS}$. Consequently, endurance was significantly improved more than 10^3 times and the variability of LRS was also improved more than 6 times (Fig. 13 & 14). The comparisons of variability and endurance with various pulse shapes are shown in Fig. 15.

4. Conclusions

For the first time, we investigated the effects of both intrinsic and extrinsic capacitance elements of RRAM. The overshoot current was minimized by optimizing SET/RESET pulse shape based on the proposed model. As a result, the endurance was significantly improved more than 10^3 times and the variability of LRS was also improved more than 6 times by the optimized pulse shape.

Acknowledgments

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References

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[3] X. Guan *et al.*, *IEEE Trans. Elec. Dev.* 59, 1172 (2012)
[4] B. Long *et al.*, *IEEE Elec. Dev. Lett.* 33, 706 (2012)

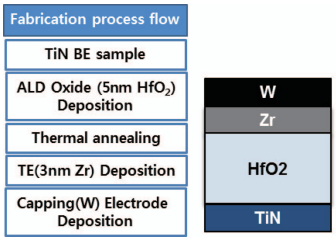

Fig. 1 Fabrication process flow and schematic diagram of RRAM device stack.

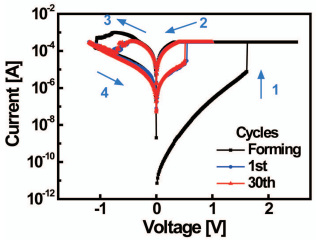

Fig. 2 Typical DC I-V switching characteristics.

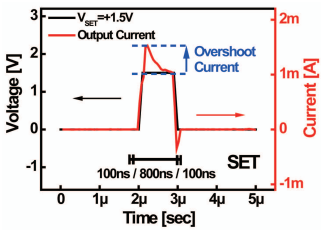

Fig. 3 Transient response during SET process. Overshoot current was observed during the rising time of SET pulse.

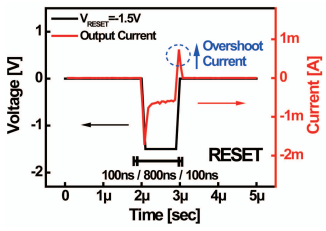

Fig. 4 Transient response during RESET process. Overshoot current was observed during the falling time of RESET pulse.

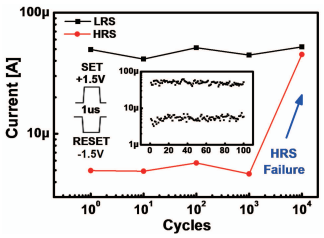

Fig. 5 Endurance of W/Zr/HfO_2/TiN device. HRS failure is observed during 10^3~10^4 cycles.

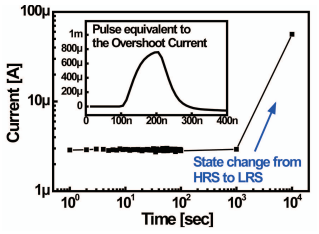

Fig. 6 Pulse equivalent to the overshoot current observed in RESET process (inset) and its effects on the RRAM cell. 10^3~10^4 cycles of equivalent pulse caused state change of the cell.

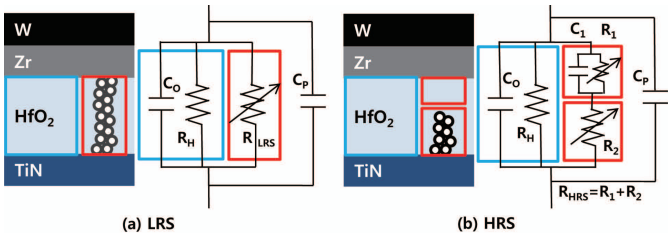

Fig. 7 Equivalent circuit model of the RRAM device with both intrinsic and extrinsic capacitance elements. (a) Equivalent circuit model for LRS. (b) Equivalent circuit model for HRS.

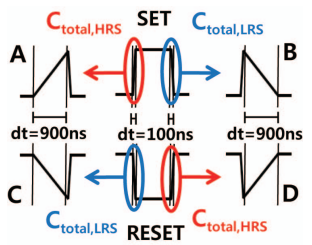

Fig. 8 Rectangular SET/RESET pulses and corresponding capacitance of each region. Length of dt was changed to control I_C.

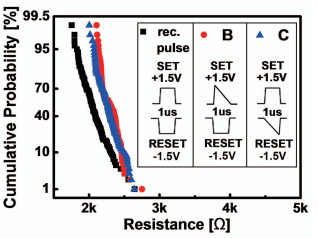

Fig. 9 Comparison of cumulative probabilities of LRS resistance with rec. pulse, B pulse and C pulse.

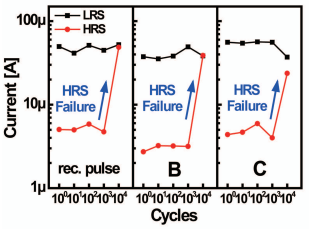

Fig. 10 Comparison of endurance with rec. pulse, B pulse and C pulse.

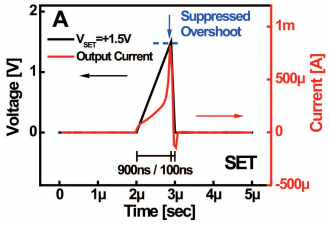

Fig. 11 Transient response of A pulse during SET process. Overshoot current was suppressed by increasing rising time of SET pulse.

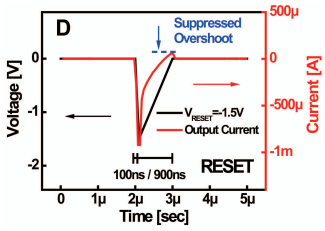

Fig. 12 Transient response of D pulse during RESET process. Overshoot current was suppressed by increasing falling time of RESET pulse.

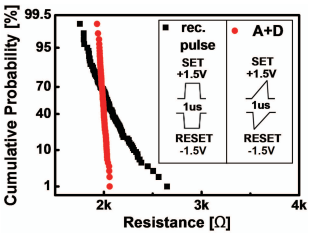

Fig. 13 Comparison of cumulative probabilities of LRS resistance with rec. pulse and A+D pulse.

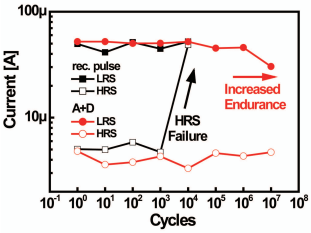

Fig. 14 Comparison of endurance with rec. pulse and A+D pulse.

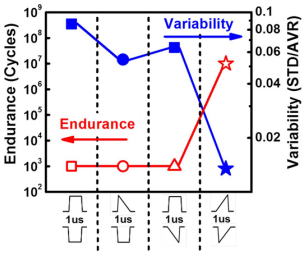

Fig. 15 Effects of pulse shapes on endurance and variability.