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Metal Oxide RRAM For Next Generation Mass Storage: 3D Vertical Architecture and Electrode/Oxide Interface Engineering

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1. Introduction

Resistive Random Access Memory (RRAM) is considered a promising candidate for future non-volatile memory application. Significant progress has been made in the past decade [1]. For instance, giga-byte size RRAM array with CMOS peripheral circuits was demonstrated recently [2]. However, to compete with ultra-high density 3D NAND FLASH [3], a technology path toward 3D stackable RRAM is required. As compared to conventional planar RRAM, stackable vertical RRAM which requires only one critical lithography step or mask is more attractive in the consideration of bit cost [4]. In this paper, we review the recent progress in the vertical RRAM including the cross-point architecture design, experimental demonstration, and analyses to provide the design guidelines. A large memory array improves area efficiency and reduces cost. An RRAM cell with higher LRS is favorable for mitigating the voltage drop on interconnect as well as reducing the programming power consumption. Utilizing the high out-of-plane resistance of single-layer graphene (SLG), an electrode/oxide interface engineering technique is developed. SLG enables the significant reduction of RESET current in RRAM and can serve as an "oxygen probe" to investigate the migration of oxygen-related defects during the electrical switching.

2. 3D Vertical RRAM Architecture Design

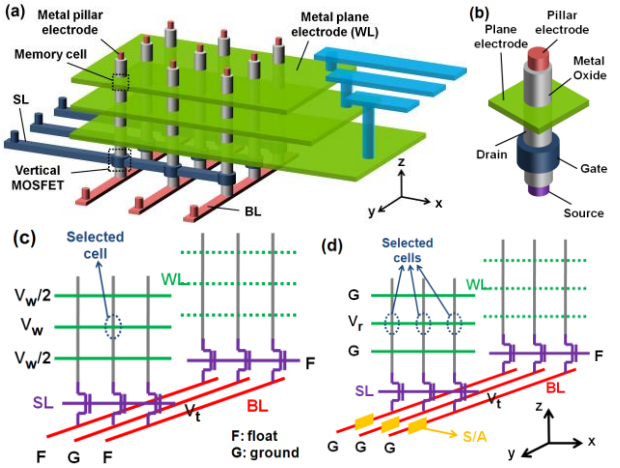


Fig. 1 (a) Schematic of a 3D vertical RRAM cross-point array. (b) The details of the structure: the switching metal oxide material is sandwiched between the plane electrode and the vertical pillar electrode. (c) and (d) show the write and read bias conditions, respectively.

Fig. 1(a) shows the 3D RRAM architecture based on vertical RRAM [5], which is constructed by the plane word-line (WL), the bit-line (BL) and the select-line (SL). A dielectric isolation layer separates the two plane electrodes (WL). The resistive switching material (such as HfO_2) sandwiched between the vertical pillar electrode and the metal plane electrode forms a RRAM cell, as illustrated in Fig.1 (b). A transistor located at the bottom of each vertical pillar serves as the BL selector. During the write operation in Fig. 1(c), a specific cell is selected: V_{write} is applied on the selected cell's WL, and $V_{write}/2$ is applied on all the unselected cells' WL to avoid unintentional writing. To select the pillar where the selected cell is located, the SL of that pillar is turned on and the corresponding BL is grounded. During the read operation in Fig. 1(d), a row of cells (on the same SL line) on one plane are read out simultaneously: V_{read} is applied on the selected cells' WL, SL that controls the selected cells is turned on, and the data of a row of cells are read out by the sense amplifiers.

3. Vertical RRAM Device Performance

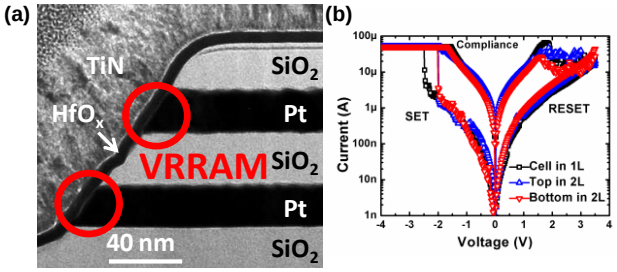


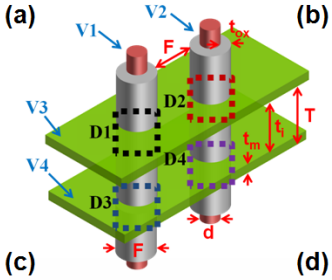
Fig. 2 (a) TEM of the double-layer (2L) HfOx-based vertical RRAM. The HfOx thickness is 5nm. (b) Typical DC I-V switching characteristics.

In order to experimentally realize such a vertical RRAM array, a cost-effective process flow is developed in [6] to fabricate single-layer (1L) and double-layer (2L, as shown in Fig. 2 (a)) HfOx-based vertical RRAMs using TiN as pillar electrodes and platinum (Pt) as plane electrodes. As shown in Fig. 2(b), the consistent switching characteristic among three samples suggests the potential of stacking multi-layer vertical RRAM using this cost-effective fabrication process. The vertical RRAM shows excellent device performances including reset current (<50μA), switching speed (~50ns), switching endurance (>10^8 cycles), half-selected read disturbance immunity (>10^9 cycles), retention (>10^5s @125°C). It is worth pointing out that electrode/oxide interface engineering using TiON layer results in low resistance state (LRS, R_{on}) up to 100k ohm and non-linear I-V characteristics. A large R_{on} from the non-linear I-V helps reduce the sneak path current, and a low interconnect resistance using metal planes as word lines reduces the undesirable voltage drop on the interconnect. As a conservative estimate in SPICE simulation, it shows that Mb-scale array without cell selector is achievable [5].

4. Demonstration of 3D Array Read/Write Schemes

The uniform electrical characteristics among the fabricated devices enable the realization of the proposed read/write schemes [7]. For a proof of concept, a fabricated cross-point 2×2 array shown in Fig. 3(a) is considered. The data pattern is pre-programmed to be D1 in LRS, D2 in HRS, D3 in HRS, and D4 in LRS. Next, the voltages applied to the pillar electrodes (V1, V2) and the plane electrodes (V3, V4) are indicated in Fig. 3(b) for the read/write operations. The read scheme aims to read out the top layer and the bottom layer, and "V/2" write scheme is applied to switch D1 between LRS

and HRS. Fig. 3(c) shows that the D1 and D4 have larger readout current, while D2 and D3 have smaller readout current, which corresponds to the data pattern. Fig. 3(d) shows that the states of the other cells remain undisturbed when D1 switches.



(b)

	V1	V2	V3	V4
Read D1&D2	0	0	0~1V	0
Read D3&D4	0	0	0	0~1V
SET D1	0	Float	-4V	-2V
RESET D1	0	Float	+4V	+2V

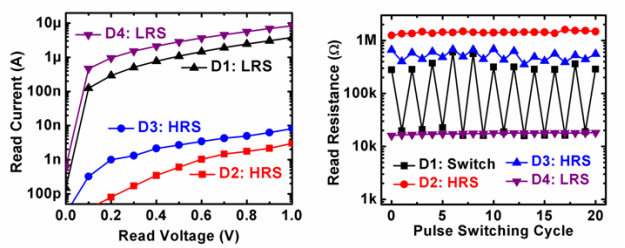
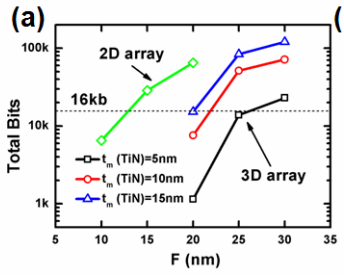


Fig. 3 (a) A skematic of 2×2 3D cross-point array. (b) Summay of operation volrages for read/write schemes (c) Measured readout current for the cells after the read operation applied. (d) Measured resistances when D1 is switched repeatedly, while the states of other cells remain unchanged.

5. Scaling Analysis of 3D Vertical RRAM

Understanding the scaling trend of each device structural element of the 3D RRAM can provide the design guidelines and tradeoffs in the future. As shown in Fig. 3(a), the 3D vertical RRAM array can be defined by the minimum dimension of the pillar electrode diameter (d), the plane electrode thickness (t_m), and the isolation layer thickness (t_i). The lithographic half-pitch, F, is defined as the pillar diameter (d) plus twice the HfOx thickness (t_{ox}, 5 nm in our experiment): $F=d+2t_{ox}$. The height (T) of one layer is: $T=t_m+t_i$.



(b)

T (for 3D) nm	F nm	A nm^2	A* nm^2
2D	13	676	676
3D (T=11)	26	38	61
3D (T=16)	22	47	75
3D (T=21)	20	56	89

A=4F^2 for 2D; A=4FT/R for 3D; $T=t_m+t_i$; $F=d+2t_{ox}$; R=30; for 16 kb array; # of layers=FR/T; A at ideal trench, A* at trench slope=89°;

Fig. 4 (a) The relation between the max total bits for an array (2D as well as 3D) and the half-pitch F for different t_m. To achieve 16k total bits, min F can be estimated at F=13 nm in 2D. (b) The integration density (cell area per bit).

The experimental results suggest that t_m can be scaled to 5 nm, and t_i scaled down to 6 nm is feasible [7]. Based on the previous experimental data, a full 3D resistor network is constructed in SPICE to study the write/read margin degradation when the pillar electrode diameter and the plane electrode thickness are scaled down [7]. Fig. 4(a) shows the tradeoffs between the total bits for an array (2D and 3D) and the litho half-pitch F for different t_m. To achieve 16-kb array, the 3D array needs a larger F than the 2D array; for the 3D array, the thinner the plane electrode is, the larger the F is required. This illustrates the tradeoffs between the plane electrode resistance and pillar electrode resistance. Fig. 4(b) shows that a 3D array has 18× higher density than a 2D array in an ideally vertical trench, or 11× higher density if assuming the trench has a slope=89°. As a guideline for 3D array design, shrinking t_m is found to be more effective for improving the storage density than shrinking F. To further enlarge the 3D array partition size, the analysis above suggests making plane metal electrode with lower resistivity materials [7].

6. Electrode/Oxide Interface Engineering

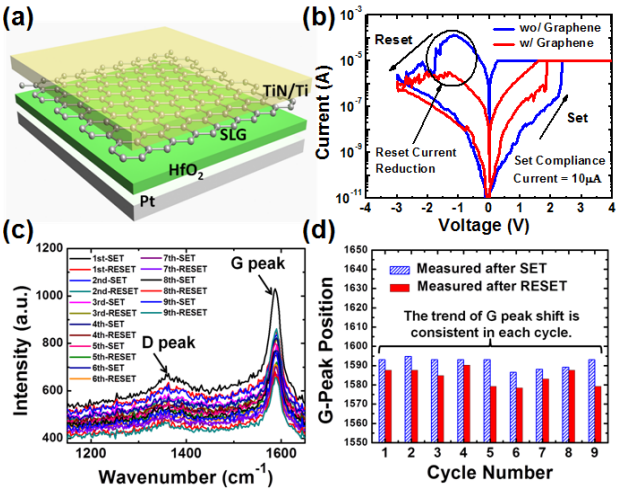


Fig. 5 (a) SLG is inserted between the top electrode and metal oxide layer. (b) Typical I-V curves of Graphene-RRAM and control sample. Significant reduction of RESET current is observed (c) 9 cycles of Raman data measured after SET and RESET cycles at the same location. (d) The position of G peak as a function of switching cycle: consitent shfit over 9 switching cycles.

Electrode/oxide interface engineering might be the next frontier for RRAM research because it may provide additional degrees of freedom to achieve desired memory characteristics. In addition to the TiON interfacial layer mentioned above, we utilize the intrinsically high out-of-plane resistance of SLG to increases LRS (> 1MΩ) in RRAM as shown in Fig. 5(a) and 5(b), which enables the substantial reduction of the RESET current by 22 times and the programming power consumption by 47 times [8]. Furthermore, such an inserted SLG allows us to monitor how the oxygen interacts with the SLG during programming by Raman spectroscopy (Fig. 5(c)). The reversible shift in G-peak signal is observed up to 9 consecutive cycles (Fig. 5(d)), which suggests the SLG may be used as an "oxygen probe" for understanding the evolution of oxygen in RRAM [9].

7. Conclusion

Recent efforts on developing 3D architectures and device engineering for RRAM are reviewed in this paper. Future research directions include the exploration of suitable material for electrodes to ensure device scalability, the design of the vertical transistors as memory array selector.

Acknowledgements

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