Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp586-587

High Performance Oxide Diode

I. P. Radu[1,2], B. Govoreanu[1], M. R. Ikram[1,2], A. P. Peter[1], K. Martens[1,2], H. Hody[1], W. Kim[1], M. Toeller[3], V. Paraschiv[1], P. Favia[1], S. Clima[1], S. De Gendt[1,2], M. Heyns[1,2], A. Stesmans[2] and M. Jurczak[1]

[1] imec Belgium, Kapeldreef 75, B-3001, Heverlee, Belgium; Phone: +32 16 28 77 19 E-mail: radu@imec.be
[2] KU Leuven, Leuven, B-3001, Belgium
[3] Tokyo Electron Limited, Tokyo 107-6325, Japan

Abstract

We report the fabrication of oxide diodes with size down to 40×40nm^2 which could be used for selector applications in high density nonvolatile memory arrays. The diodes consist of VO_2 and TiO_2 while the electrodes are TiN. The diodes show current density up 10^5A/cm^2 and ideality factors less than 2.3. Turn-on time is shorter than 5ns, and cycling endurance higher than 10^9cy.

1. Introduction

The major roadblock for the implementation of resistive memory in multilayer high density arrays is the lack of an appropriate selector device. The selector has to limit the leakage current through unselected memory cells in arrays. Diodes are the most studied devices for this application.

Oxide diodes can be built either as p-n junctions or as Schottky diodes. While many n-type semiconducting oxides are known (TiO_2 is the most prominent example), very few p-type oxides are available and typically have a large band gap which results in devices with a large turn-on voltage and low current [1]. Schottky diodes where an oxide is sandwiched between two metals have been investigated extensively [2]. Schottky barriers are easily destroyed by bias stress and often use metals with a high work function such as Pt, which are not CMOS compatible. In these devices it is also difficult to control between diode behavior and non-volatile resistive switching [3].

VO_2 is reported to have a work function of ~5.2eV [4] and be p or n doped depending on the production conditions.

2. Results and discussion

Material and device fabrication

The devices are fabricated on 300mm Si wafers. The electrodes have a cross-bar geometry (Fig.1). TiN bottom electrodes (BE) are patterned and planarized on SiO_2 isolation. VO_2 [5] and TiO_2 [6] are deposited via atomic layer deposition (ALD). The TiN top electrode is sputtered and the whole stack is patterned with dry etching stopping on BE. There are 2 types of active stacks investigated: 1) ALD VO_2 followed by a crystallization anneal and ALD of TiO_2; 2) ALD TiO_2 followed by the deposition of VO_2 and the anneal. The anneal was the same for all stacks. A TEM cross-section of a device is presented in Fig. 2 showing that both the VO_2 and the TiO_2 are fully crystalline. X-ray diffraction (XRD) patterns of the 2 types of stacks are shown in Fig. 3. Independent of the order of the 2 oxides in the stack, only one XRD peak (other than TiN) is observed. This peak is compatible with the plane (011) of VO_2 and (110) of rutile TiO_2.

Electrical characterization

Typical rectifying behavior is shown in Fig. 4 for both types of stacks. Upon reversing the stack, the polarity of the forward bias changes accordingly. Devices fabricated with the VO_2/TiO_2 stack show area scaling of the current only at large current while those with the TiO_2/VO_2 stack show perfect area scaling at all currents levels. This can be explained by the fact that the VO_2 has a relatively low resistivity and the whole oxides stack is present under the top electrode. This creates an extra conduction path which is visible only at low currents.

The diode factor is lower than 2.3 for all stacks, demonstrating excellent diode behavior, better than typical oxide diodes [1]. The current density increases with decreasing thickness of the TiO_2 and is as high as 10^5A/cm^2 at 2V for devices with 4nm TiO_2/9nm VO_2.

Devices show good temperature stability and rectification (Fig. 5) even though the VO_2 likely undergoes a metal to insulator transition around 60 ºC.

Pulsed measurements reveal that the diode response time is less than 5ns (Fig. 7) suggesting that the rectification is largely arising from the large work function of VO_2. Pulsed endurance testing shows cycling to at least 10^9 cycles (Fig. 8). Constant voltage stress measurements (Fig. 9) show little change in current levels for 1000s (assuming 10ns cycles, this translates into an endurance better than 10^{11}cy).

3. Conclusions

We have demonstrated high performance VO_2/TiO_2 diodes with dimensions as small as 40×40nm^2 and current density as high as 10^5A/cm^2 at 2V. The diodes show response times faster than 5ns. We report for the first time oxides diodes with endurance higher than 10^9 cycles.

Acknowledgements

We acknowledge the imec industrial affiliation program and a joint development program with TEL Japan. IPR and KM acknowledge financial support from FWO Vlaanderen. IPR acknowledges a Marie Curie Reintegration Grant. We thank Nico Jossart for acquiring the SEM images.

References

[1] M. J. Lee *et al.*, IEDM Tech. Digest (2007) 771.
[2] Y. C. Shin *et al.*, Appl. Phys. Lett. **92** (2008) 162904.
[3] J. J. Huang *et al.*, Appl. Phys. Lett. **96** (2010) 262901.
[4] K. Martens *et al.*, J. Appl. Phys. **112** (2012) 124501.
[5] A. P. Peter *et al.*, ECS J. Solid State Sci. Technol. **1** (2012) 169.
[6] M. Popovici *et al.* Microel. Eng. **88** (2011) 1517.

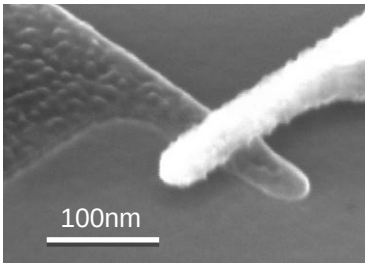

Fig. 1: SEM image of a cross-bar device.

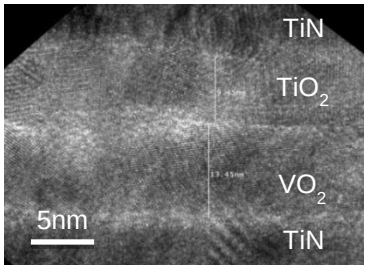

Fig. 2: TEM cross-section of a device.

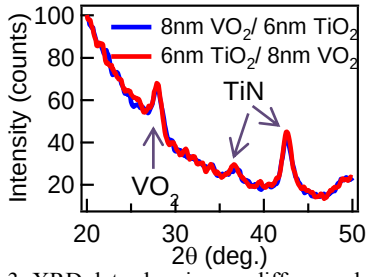

Fig. 3: XRD data showing no difference between stacks with VO_2/TiO_2 and TiO_2/VO_2.

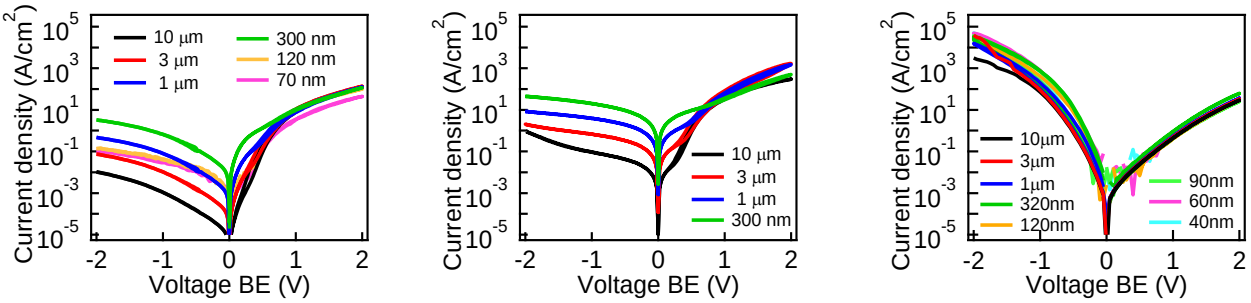

Fig. 4: Current density vs. bias for devices with 9nm VO_2/12nm TiO_2 (left), 9nm VO_2/9nm TiO_2 (middle) and 4nm TiO_2/9nm VO_2 (right). Perfect area scaling of current is observed for devices with 4nm TiO_2/9nm VO_2.

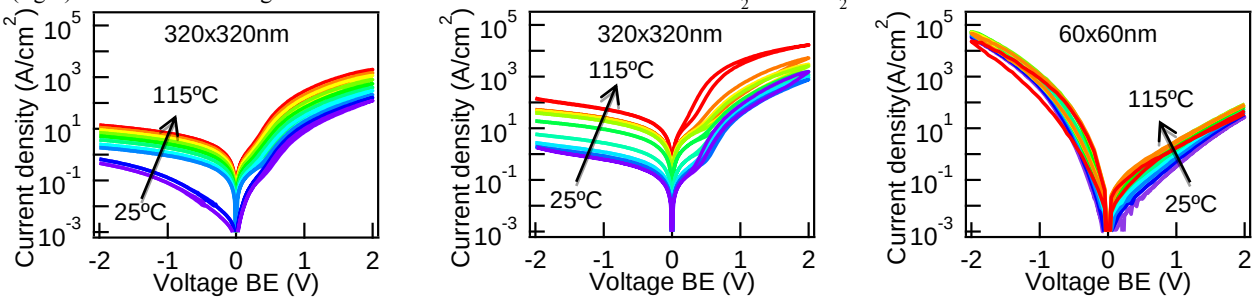

Fig. 5: Temperature dependence of the current density vs. bias for devices with 9nm VO_2/12nm TiO_2 (left), 9nm VO_2/9nm TiO_2 (middle) and 4nm TiO_2/9nm VO_2 (right). Device size is marked on the figure. Temperature is increased in steps of 10ºC.

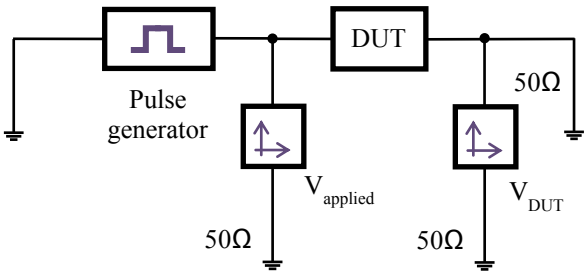

Fig. 6: Sketch of the pulsed measurement setup used to acquire data in Fig 7and 8.

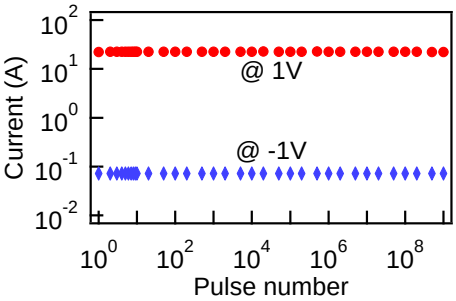

Fig. 8: Endurance test of a 10x10µm^2 device with 9nmVO_2/9nm TiO_2 over 10^9 cycles.

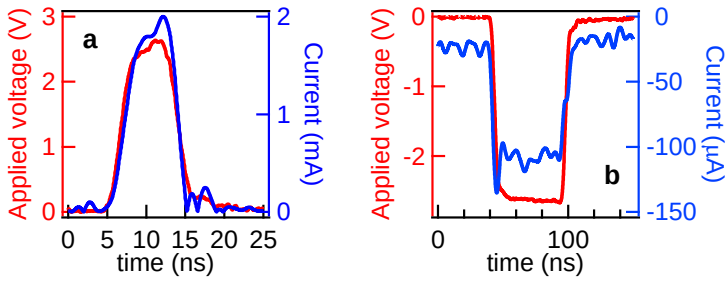

Fig. 7: Pulse shapes in forward (a) and reverse (b) bias for devices with 9nmVO_2/9nm TiO_2 showing that the diodes turn on in less than 5 ns.

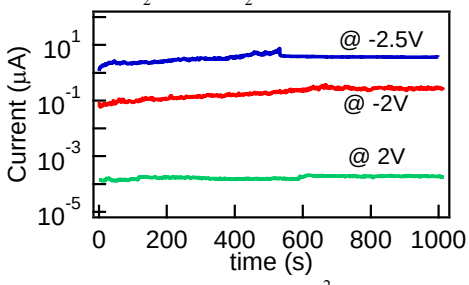

Fig. 9: Stress test of a 65x65nm^2 device with 4nmTiO_2/9nm VO_2 showing little change in current levels over 1000s.