
Thermal and Plasma Treatments for Improved (Sub)-1nm EOT Planar and FinFET-based RMG High-k Last Devices and Enabling a Simplified Scalable CMOS Integration Scheme

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Abstract
We report on aggressively scaled RMG-HKL planar and multi-gate FinFET-based devices, systematically investigating the impact of post high-k deposition thermal (PDA) and plasma (SF6) treatments on high-k dielectric physical thickness and EOT. Indeed, Figs.14a,b show similar EOT-JG, VT nFETs are obtained by depositing the n-EWF metal after the HfO2 growth [9] or following the SF6 removal of the p-EWF/barrier metals from NMOS areas. No impact on device properties from a longer HfO2 exposure to SF6 (similar VT, opposite occurs upon exposure of HfO2 to SF6). Similar trends are observed for FinFETs planar FETs built with PDA, with their smaller |ΔVT| and |Δσ| at high |ID|, indicating less charge trapping into bulk defects that do not contribute to BTI and N assessment of reduced bulk defects presence. LF-noise analyses show in Figs.10a,b improved normalized input-referred noise spectral density values (∼3-4.5× lower SV f vs. reference) with PDA. In agreement with BTI results, further gain is obtained for FinFETs with (100) fin sidewalls, with all devices largely following 1/f noise behavior (Fig.10c). Proportionality of the normalized current noise spectral density (S I/f) with (g m/ID)2 for reference and fluorinated devices (Fig.10d), at lower |ID|, points towards carrier number fluctuations or oxide trapping in OT, consistent with mobility fluctuations at the origin of LF-noise, whereas that does not seem to be always the case with PDA.

Conclusions
Reduced |ΔVT| and noise values achieved by using PDA and a SFx plasma after HfO2 growth in planar and FinFET devices, without EOT penalty. SFx also improves mobility and reduces Nbd for Wfin≥5nm, allowing a simplified, highly scalable dual-EWF metal CMOS scheme suitable for both device architectures. Substantially improved NBTI lifetime and hot-carrier immunity for (sub-)1nm EOT is obtained by bulk defects reduction with PDA.

References
Fig. 1 – Schematics of the process flow used for fabrication of replacement metal gate/high-k last (RMG-HKL) planar and multi-gate FinFET-based devices.

Fig. 2 – Schematics of gate stacks (as-deposited) evaluated in this work for both planar (bottom right, TEM) and FinFET-based (top) RMG-HKL devices.

Fig. 3 – PDA after HfO2 growth results in lower PMOS \( V_{th} \) growth while the opposite occurs with high-k exposure to SF6. Similar trends are seen for planar (a) and FinFET devices (a,b); ITP in (b), but with smaller \( V_{th} \) shifts for the latter.

Fig. 4 – Slight mobility improvement with SF6 for FinFETs and planar FETs (no EOT penalty). PDA impacts high-field values mostly in planar.

Fig. 5 – Interface trap density \( (N_t) \) estimated from charge pumping is higher for FinFETs with (110) vs. (100) fin vertical sidewalls (SW) and in comparison to planar bulk devices. In all cases, F incorporation in the stack by a SF6-plasma results in reduced \( N_t \) whereas PDA increases it.

Fig. 6 – Use of a SF6-plasma is effective to keep reduced \( N_{trm} \) \( W_{fin} \) for devices with (110) (100) sidewalls. A less steep \( N_{trm} \) vs. \( W_{fin} \) slope with SF6 and also PDA indicates less defects at fin corners in both cases.

Fig. 7 – NBTI lifetime is significantly improved with PDA for planar FETs, corresponding to lower total effective trapped charge density values and to recoverable (R) and permanent (P) degradation components with a less steep slope vs. \( \Delta V_{th} \).

Fig. 8 – Similarly to planar, also substantial NBTI improvement is obtained in FinFETs, a more modest gain with SF6. BTI degradation is reduced for (100) vs. (110) fin sidewalls and for narrower fin devices.

Fig. 9 – HC degradation of FinFET devices with (100) fin sidewalls is reduced by including PDA in the flow. The smaller \( I_d \) degradation (\( \Delta V_{th} \)) or \( \Delta V_{th} \) at high \( V_{th} \) corresponds thus mostly to less charge trapping into bulk defects and to no significant impact from \( N_{trm} \).

Fig. 10 – Normalized \( S_{res} \) values for RMG-HKL devices are in line with the ITRS \( 1/f \) noise roadmap (planar data in (a)). Noise is correspondingly reduced with EOT, for both planar and narrow-fin devices, and (100) fin sidewalls are beneficial (b,c,d) for examples of LF-noise spectra and the \( S_{res} \) correlation with \( \Delta V_{th} \), respectively.

Fig. 11 – Simplified dual-EWF metal gate/high-k CMOS scheme, planar and FinFET compatible, with a SF6-plasma removing the p-EWF/barrier metals from the NMOS areas.

Fig. 12 – XPS analyses show F incorporation into HfO2 upon exposure to a SF6-plasma. Hf-F bonds are mainly present at the surface, with only limited amount of F detected in the bulk of the HfO2.

Fig. 13 – An optimized clean after strip is required to be able to use a SF6-plasma to remove metals from inside gate trenches without impacting the physical thickness of the high-k dielectric underneath, and with F incorporated in it (=> \( N_{trm} \) reduction).

Fig. 14 – a,b) Similar \( V_{th} \) and \( EOT \) are obtained for nFETs built with the n-EWF metal deposited after HfO2 growth or after using the SF6-based CMOS process. SF6 pre-etch has no impact on devices (a,b) and circuits (RO in (d)). b) shows that PDA significantly reduces \( J_d \) at a given \( V_{th} \) for nFETs, with smaller \( N_{trm} \) for pFETs (c).