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Charge neutrality level shift in the Bardeen limit of Fermi-level pinning at atomically flat Ge/metal interface

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Abstract

In this work, we investigated the Fermi level pinning (FLP) at metal/Ge interface formed on atomically flat Ge(111) surface. The effective charge neutrality level ϕ_{CNL} is shifted by 0.1 eV from that of metal/Ge interface formed on rough surface. The ϕ_{CNL} shift associated with interface Ge structure should be considered to discuss the FLP at metal/Ge interface in addition to S parameter.

1. Introduction

Fermi level pinning (FLP) at the metal/semiconductor interface is generally described as follows,

$q\phi_{bn} = S\,(q\phi_m - q\chi) + (1 - S)\,(q\phi_{CNL} - q\chi)$,

where $q\phi_{bn}$ is the Schottky barrier height (SBH) to conduction band edge of semiconductor, $q\phi_m$ is the work function of metal, $q\chi$ is electron affinity of semiconductor, S is $\partial\phi_{bn}/\partial\phi_m$, and $q\phi_{CNL}$ is effective charge neutrality level. Therefore, S and $q\phi_{CNL}$ are critical for understanding the FLP. In the case of Ge, strong FLP (S ~ 0 (Bardeen limit)) close to valence band edge of Ge ($q\phi_{CNL} \sim q\chi + E_g$) has been reported at metal/Ge interface [1,2]. The origin of strong FLP has not been identified, because it is inferred that the metal/Ge interface still includes extrinsic FLP factors (ex. defects [3] and/or disorder induced gap states [4]).

Recently, we successfully formed the atomically flat Ge(111) surface by H_2 annealing process [5]. It is expected that the extrinsic FLP factors might be well eliminated by forming the well-defined structure. Then, the objective of this work is to study the FLP of metal/Ge interface employing the atomically flat surface.

2. Experimental

We prepared two kinds of surface structures on n-type Ge (111) substrates. One was chemically cleaned surface, and the other was atomically flat surface formed by H_2 annealing after chemical cleaning. The step & terrace structure was formed by annealing in H_2 ambient at 650°C for 15 min. The detail of H_2 annealing is described elsewhere [5]. **Fig. 1** shows the AFM images of chemically cleaned Ge(111) surface and H_2 annealed one. The step & terrace on H_2 annealed Ge(111) surface are clearly observed.

The Ge Schottky diodes were fabricated by thermal evaporation of several metals (Ag, Al, Cu, Co, Au and Ni) on both chemically-cleaned Ge(111) substrate and H_2 annealed one. Both electrode area and peripheral length was changed from 1.2 to 8.6 x 10^4 μm^2 and from 4.5 to 11 x10^3 μm respectively to eliminate the peripheral leakage current.

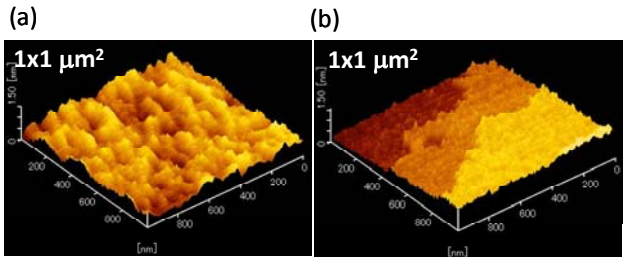

Fig. 1 AFM images of (a) chemically-cleaned and (b) H_2 annealed Ge(111) surface. Roughness root mean square values at 1 x 1μm^2 are 0.15, and 0.20. Step & terrace structure is observed on the H_2 annealed Ge(111) surface. Almost step is composed by single step which is equal to be 0.326 nm.

3. Results and Discussion

All n-Ge/metal junctions fabricated in this work showed Schottky characteristics irrespective of the work function of metals. However, in most metal cases, the off-leakage current of H_2 annealed sample was definitely

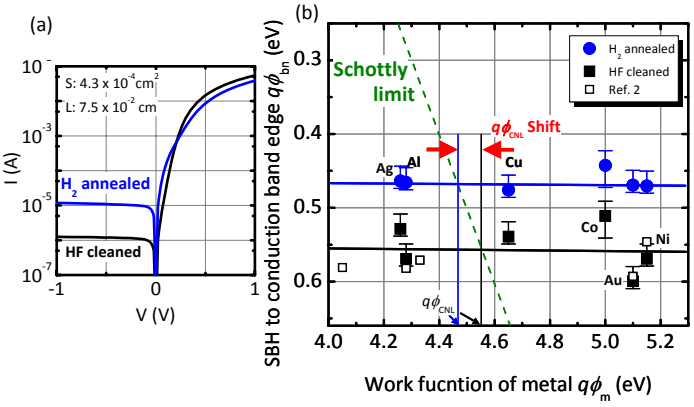

Fig. 2(a) I-V characteristics of Au/n-Ge Schottky junction formed on H_2 annealed Ge(111) and HF cleaned Ge (111). **(b)** Evaluated $q\phi_{bn}$ as a function of work function of metals. The broken line denotes the Schottky limit. $q\phi_{CNL}$ is estimated from the intersection of the Schottky limit line with experimentally obtained line. Thanks to the Bardeen limit of S paramerer, it is clearly observed that $q\phi_{CNL}$ is shifted by surface flattening.

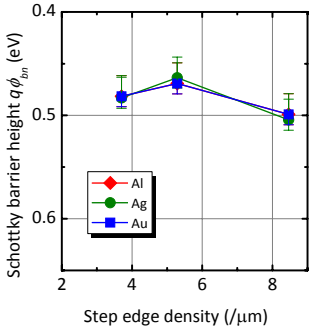

Fig. 3 Schottky barrier height at various metal/n-Ge interface as a function of surface step density. Estimated $q\phi_{bn}$ does not reduced with increasing step edge density, which indicates that the local $q\phi_{bn}$ reduction due to the step edge does not occur.

larger than chemically cleaned one (**Fig. 1 (a)**). The SBH value of metal/n-Ge interface was estimated from the I-V characteristics. Saturation current I_s in each diode was estimated by extrapolating the off-leakage current to V = 0, and then the saturation current density J_s was evaluated from the peripheral length dependence of electrode on I_s to eliminate the peripheral leakage. Then, the exact $q\phi_{bn}$ was calculated from the J_s with the following equation,

$$q\phi_{bn} = k_B T \ln\left(\frac{AT^2}{J_s}\right),$$

where A is the Richardson constant (67 A/cm^2/K^2 for n-Ge). **Figure 2(b)** shows the evaluated $q\phi_{bn}$ in various metals. Here, the work functions reported in the literature was assumed[6]. Although the Bardeen limit is still observed even on the H_2 annealed samples, it should be noted that its $q\phi_{CNL}$ is shifted by 0.1 eV from that of metal/Ge interface formed on chemically cleaned Ge(111) one.

Since the H_2 annealed Ge(111) surface consists of the step and terrace as shown in Fig. 1(a), it is concerned that the step edge might induce a local leakage path and cause apparent $q\phi_{bn}$ lowering. We investigated the step density dependence of Ge(111) substrate on $q\phi_{bn}$ by changing the off-angle of Ge(111) substrate. On the H_2 annealed Ge (111) surface with off-angle of 0.07°, 0.10° and 0.16°, the step density was estimated to be 3.7, 5.2 and 8.3 step/μm by AFM measurement, respectively, which implies the step density is simply determined by the off-angle of substrate at 650°C without the step bunching formation observed on Si(111). However, possible $q\phi_{bn}$ lowering caused by an increase of leakage current at step edge was not observed as shown in **Fig. 3**. Namely, it is suggested that the $q\phi_{bn}$ is determined on the terrace, and that $q\phi_{CNL}$ of metal/Ge interface formed on H_2 annealed Ge(111) is actually different that on chemically cleaned one.

Finally, $q\phi_{CNL}$ at metal/Ge interface is discussed. Tersoff has proposed that $q\phi_{CNL}$ at metal/semiconductor interface is close to the charge neutrality level defined in bulk semiconductor [7]. The charge neutrality level of bulk Ge are theoretically estimated to be 4.48 [8] and 4.63eV [9], which are in a good agreement with the previous results obtained experimentally [1,2]. However, thanks to the small S parameter of metal/Ge interface, it is clarified that $q\phi_{CNL}$ at metal/Ge interface is definitely shifted on atomically flat Ge surface as schematically shown in **Fig. 4**. Namely, $q\phi_{CNL}$ at metal/Ge interface is determined not only by bulk characteristics of semiconductor but also by surface

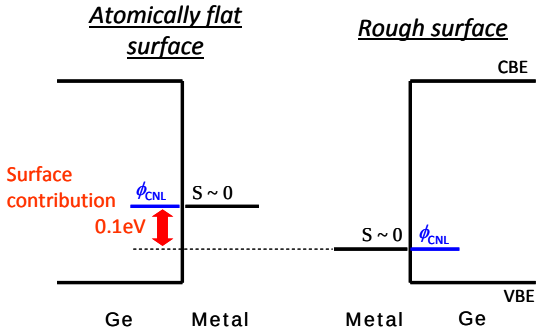

Fig. 4 Schematics of $q\phi_{CNL}$ at metal/Ge interface. The result of this work clearly indicates that the $q\phi_{CNL}$ is affected by interface structure. Considering the S parameter is almost 0 both on atomically flat surface and rough one, it is expected that the origin of FLP is same but its energy level (charge neutrality level in bulk Ge) is modulated by surface structural factor.

microstructure.

It is recently reported that $q\phi_{bn}$ at epitaxial Fe_3Si/Ge interface is reduced down to 0.46 eV [10]. They speculated that the FLP is alleviated by the passivation of extrinsic FLP factors (defect and dangling bond) due to the epitaxial interface formation [11]. However, considering the result of this work, it is possible that the reduction of $q\phi_{bn}$ at epitaxial metal/Ge interface is also explained by $q\phi_{CNL}$ shift associated with the interface microstructure of Ge. Therefore, we should take care of both S parameter and $q\phi_{CNL}$ to discuss the SBH modulation even in the case of metal/Ge interface.

4. Conclusion

It has been found for the first time that $q\phi_{CNL}$ at metal/Ge interface is shifted by 0.1 eV in Berdeen limit of FLP on atomically flat Ge (111) surface. This fact clearly indicates that $q\phi_{CNL}$ is determined not only by the bulk characteristics of Ge but also by the interface structure. Therefore, to discuss the SBH modulation at metal/Ge interface from the viewpoint of FLP, $q\phi_{CNL}$ in addition to S parameter should be carefully taken into account.

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References

[1] A. Dimoulas, et al., Appl. Phys. Lett. **89** (2006) 252110. [2] T. Nishimura, et al., Appl. Phys. Lett. **91** (2007) 123123. [3] W. E. Spicer, et al., J. Vac. Sci. Technol. B **6** (1988) 1245. [4] H. Hasegawa and H. Ohno, J. Vac. Sci. Technol. B **4** (1986) 1130. [5] T. Nishimura, et al., Appl. Phys. Express. **5** (2012) 121301. [6] H. B. Michaelson, J. Appl. Phys. **48** (1977) 4729. [7] J. Tersoff, Phys. Rev. Lett. **52** (1984) 465. [8] J. Tersoff, J. Vac. Sci. Technol. B **4** (1986) 1066. [9] M. Cardona and N. Chiristensen, Phys. Rev. B **35** (1987) 6182. [10] K. Yamane, et al., Appl. Phys. Lett. **96** (2010) 162104. [11] Kasahara, et al., Phys. Rev. B **84** (2011) 205301.