Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp622-623

Germanium-Tin Tunneling Field-Effect Transistor: Device Design and Experimental Realization

Yue Yang, Pengfei Guo, Wei Wang, Xiao Gong, Lanxiang Wang, Kain Lu Low, Genquan Han, and Yee-Chia Yeo*

Dept. of Electrical & Computer Engineering, National University of Singapore (NUS), 117576 Singapore.
* Phone: +65 6516-2298, Fax: +65 6779-1103, E-mail: yeo@ieee.org

Abstract
Germanium-tin (GeSn) can have small and direct bandgap (E_G) and is promising for application in pTFET. GeSn pTFET is studied by simulation. A first prototype is also experimentally realized using a sub-450 °C gate-first process, and high drive current was obtained. This is attributed to direct BTBT, high hole mobility in the GeSn channel, and the formation of heavily doped n^+ source.

1. Introduction

As complementary metal-oxide-semiconductor (CMOS) is scaled down towards the end of the technology roadmap, alternative devices are proposed to overcome the subthreshold swing (*S*) limitation (60 mV/decade at room temperature) to enable ultra-low supply voltage V_{DD}. Tunneling field-effect transistor (TFET), which exploits gate-modulated band-to-band tunneling (BTBT), is a promising candidate (Fig. 1). Research efforts have focused on improving the drive current of TFETs, for which small bandgap E_G materials are required (Fig. 2) [1]-[12]. For n-channel TFET (nTFET), III-V materials were used to achieve drive current above 100 μA/μm [3-6]. The direct BTBT and high electron mobility in III-V materials helped. However, for p-channel TFETs (pTFET), materials used are mainly the group IV materials (Si, Ge, and SiGe [7-10]), and more research is needed to enhance the tunneling current for pTFETs.

For a pTFET in the on-state (Fig. 3), BTBT of electrons from the channel to the n^+ source occurs, leaving behind holes that are transported towards the p^+ drain. To enhance the tunneling current in pTFETs, both high BTBT probability and high hole mobility are desired. Germanium-tin (GeSn) is a promising and new substrate material for pTFETs as it can offer high BTBT probability due to a smaller and direct bandgap ($E_{G,\Gamma}$) (Fig. 4) as well as higher hole mobility as compared to Ge [13-14]. In addition, the low activation temperature (400 °C) for phosphorus in GeSn [15] favors the formation of shallow n^+ junction and avoids gate stack degradation due to high thermal budget in a gate-first process.

2. Simulation Assessment

The E_G of $Ge_{1-x}Sn_x$ can be tuned by adjusting the Sn composition *x*. As *x* increases, both the direct $E_{G,\Gamma}$ at Γ-point and indirect E_G ($E_{G,L}$) at L-point reduce, and $Ge_{1-x}Sn_x$ transits from indirect to direct E_G material at *x* of ~0.11 (Fig. 4). Simulated I_{DS}-V_{GS} characteristics for $Ge_{1-x}Sn_x$ pTFET with various *x* [Fig. 5(a)] show that I_{DS} increases with increasing *x*, mainly due to the reduced $E_{G,\Gamma}$. The simulated I_{DS} is the total tunneling current contributed by both direct BTBT (Γ-Γ BTBT) and indirect BTBT (Γ-*L* BTBT).

The tunneling current components in $Ge_{0.96}Sn_{0.04}$ pTFET and $Ge_{0.88}Sn_{0.12}$ pTFET are shown in Fig. 5(b) and (c), respectively. It can be observed that the onset voltage of Γ-Γ BTBT becomes smaller than that of Γ-*L* BTBT with increasing *x*. The magnitude of Γ-Γ BTBT current is much higher than that of Γ-*L* BTBT current due to the higher tunneling probability across a direct bandgap without a change in momentum. Once Γ-Γ BTBT occurs with sufficient V_{GS}, it quickly dominates the I_{DS}. Therefore, for $Ge_{1-x}Sn_x$ pTFETs with $x \geq 0.11$, the *S* becomes much steeper since I_{DS} is dominated by Γ-Γ BTBT in the entire range of V_{GS}. I_{DS} in $Ge_{1-x}Sn_x$ pTFETs at various V_{DD} windows (0.2~0.6 V) is calculated for a fixed I_{off} = 0.1 nA/μm, and the contour plot versus *x* and V_{DD} is shown in Fig. 6. An I_{DS} of 300 μA/μm can be achieved by $Ge_{0.86}Sn_{0.14}$ pTFETs at V_{DD} = 0.6 V.

3. Experimental Realization

Fig. 7 shows a process flow for fabricating GeSn pTFETs. After epitaxial growth of GeSn film (~146 nm) on n-type (100) Ge substrate, phosphorus (P) well implant was performed and activated at 450 °C for 3 minutes. Si_2H_6 surface passivation was carried out at 370 °C after pre-gate cleaning and native oxide removal by SF_6 treatment. TaN/HfO_2 gate stack was formed. BF_2^+ and P^+ implants were used to form drain and source, respectively, and were activated together at 400 °C for 5 minutes. Ni(GeSn) metal contacts were formed. The top-view SEM image of the fabricated GeSn pTFET is shown in Fig. 8(a). TEM images show the n^+ source formation [Fig. 8(b)] and the TaN/HfO_2 stack formed on an ultra-thin SiO_2/Si cap on $Ge_{0.958}Sn_{0.042}$ [Fig. 8(c) and (d)].

SIMS profiles (Fig. 9) confirm that about 20 nm phosphorus-rich or n^+ GeSn layer is formed underneath Ni(GeSn) as n^+ source region. The I_{DS}-V_{GS} and I_{DS}-V_{DS} of a typical GeSn pTFET with a gate length of 4 μm are shown in Fig. 10(a) and (b), respectively. Good transfer and output characteristics are observed, and an I_{DS} of 28 μA/μm is achieved at V_{GS} = V_{DS} = - 2 V. Low temperature device characteristics were investigated [Fig. 11(a)]. With decreasing temperature, the leakage floor is lowered, allowing the region with steeper *S* to be more visible. Drive current is weakly dependent on temperature, as expected. When the temperature is below 240 K, I_{DS} is reduced due to the increase in E_G. The Arrhenius plots in Fig. 11(b) show that, for V_{DS} = -0.05 V, I_{off} is dominated by Shockley-Read-Hall generation, while at V_{DS} = -1 V, drain-side BTBT dominates the I_{off}.

4. Device Optimization

Although the drive current in homo-GeSn pTFET is high, it has large leakage current floor caused by the severe thermal generation and drain-side BTBT due to small E_G of GeSn. Heterojunction, such as $Ge_{0.96}Sn_{0.04}$/$Si_{0.12}Ge_{0.77}Sn_{0.11}$ with a type-II staggered band alignment, could be employed to suppress leakage current (Fig. 12). In addition, drain engineering, such as drain region underlap with gate, could be used to suppress drain side BTBT.

5. Conclusions

The performance of $Ge_{1-x}Sn_x$ pTFETs is assessed by simulation. Planar $Ge_{0.958}Sn_{0.042}$ devices were experimentally realized. Good device characteristics were obtained, which is attributed to enhanced direct BTBT, high hole mobility in the GeSn channel, and the formation of heavily doped n^+ source junction at low temperature. The performance can be improved with further device architecture or process optimization.

Acknowledgments. The authors acknowledge discussions with Prof. B. Cheng of the Institute of Semiconductors, Chinese Academy of Sciences, China. Y.-C. Yeo acknowledges support from the National Research Foundation under Grant NRF-RF2008-09.

References

[1] T. Krishnamohan *et al*., *IEDM 2008*, pp. 947.
[2] S. H. Kim *et al*., *VLSI 2009*, pp. 178.
[3] S. Mookerjea *et al*., *IEDM 2009*, pp. 949.
[4] G. Dewey *et al*., *IEDM 2011*, pp. 0785.
[5] D. K. Mohata *et al*., *IEDM 2011*, pp. 781.
[6] G. Zhou *et al*., *IEDM 2012*, pp. 777.
[7] F. Mayer *et al*., *IEDM 2008*, pp. 163.
[8] D. Leonelli *et al*., *JJAP 50*, pp. 04DC05, 2010.
[9] K. Jeon *et al*., *VLSI 2010*, pp. 48.
[10] A. Villalon *et al*., *VLSI 2012*, pp. 49.
[11] Y. Yang *et al*., *IEDM 2012*, pp. 379.
[12] H. Riel *et al*., *IEDM 2012*, pp. 391.
[13] G. Han *et al*., *IEDM 2011*, pp. 402.
[14] S. Gupta *et al*., *IEDM 2011*, pp. 398.
[15] L. Wang *et al*., *EDL 33*, pp. 1529, 2012.

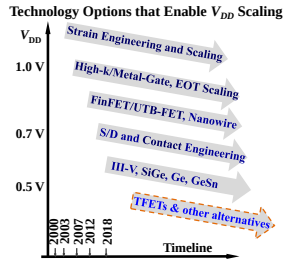

Fig. 1. With continuous scaling of device dimensions and V_{DD}, new technology options are needed for ultra-low V_{DD} and power applications.

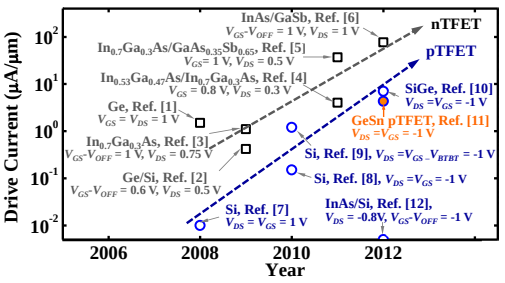

Fig. 2. Recent reports of nTFETs and pTFETs show that small E_G materials and hetero tunneling junction are needed to achieve high I_{on}. I_{on} in nTFETs has been improved by incorporating III-V materials, however more efforts are required to improve I_{on} of pTFETs.

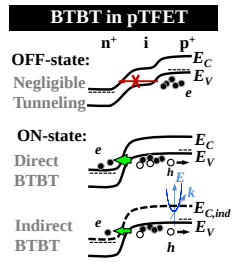

Fig. 3. BTBT is negligible at off-state. Direct/ indirect BTBT occurs when pTFET is at on-state.

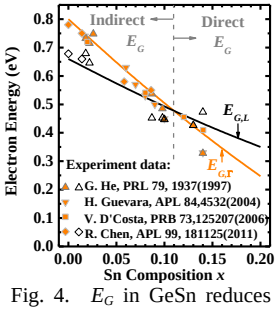

Fig. 4. E_G in GeSn reduces with increasing Sn composition. Direct E_G occurs when x is larger than 0.11.

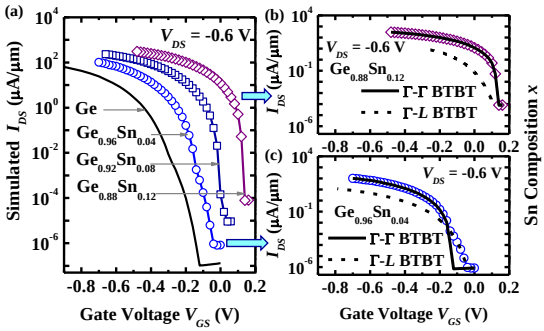

Fig. 5. (a) Simulated I_{DS}-V_{GS} characteristics of $Ge_{1-x}Sn_x$ TFETs with various x (x = 0, 0.04, 0.08, and 0.12). Current components of Γ-Γ BTBT and Γ-L BTBT for (b) $Ge_{0.96}Sn_{0.04}$ and (c) $Ge_{0.88}Sn_{0.12}$ pTFETs, respectively.

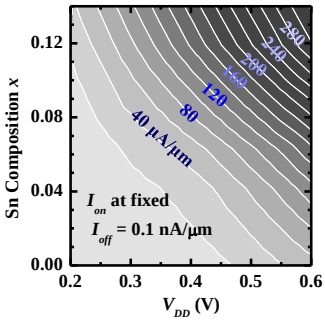

Fig. 6. Contour plot of I_{on} with various x with V_{DD} ranging from 0.2~0.6 V. I_{on} of 300 μA/μm can be achieved at V_{DD} = 0.6 V for $Ge_{0.86}Sn_{0.14}$ pTFET.

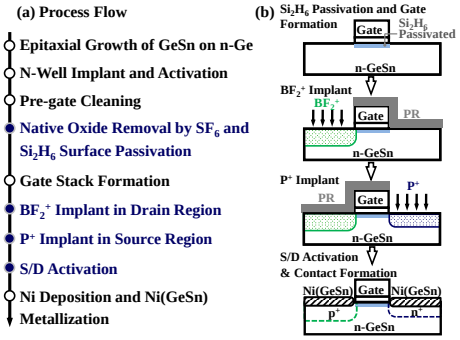

Fig. 7. (a) Process flow for fabricating planar GeSn pTFETs. (b) 2D schematics of structures after key process steps: Si_2H_6 passivation, BF_2^+ drain implant, P^+ source implant, and Ni(GeSn) formation after S/D activation.

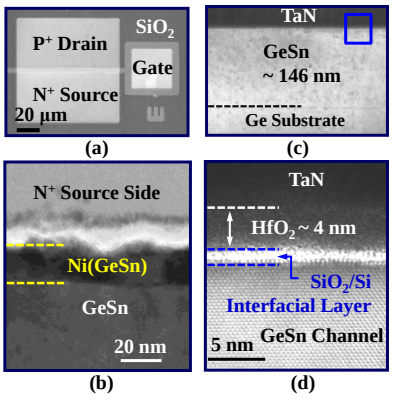

Fig. 8. (a) SEM image of a GeSn pTFET. TEM for (b) source and (c) (d) gate stack.

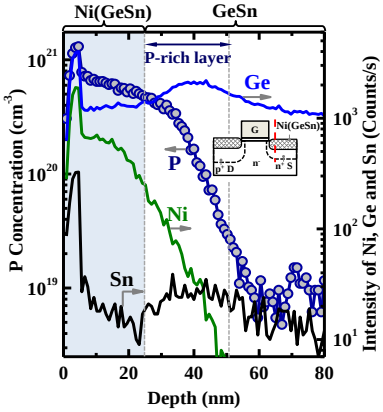

Fig. 9. SIMS profiles of Ge, P, Ni and Sn at N^+ source side of a GeSn pTFET.

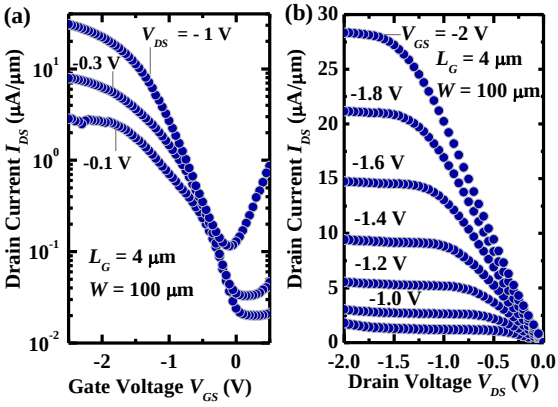

Fig. 10. (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristic of a typical GeSn pTFET with a gate length of 4 μm.

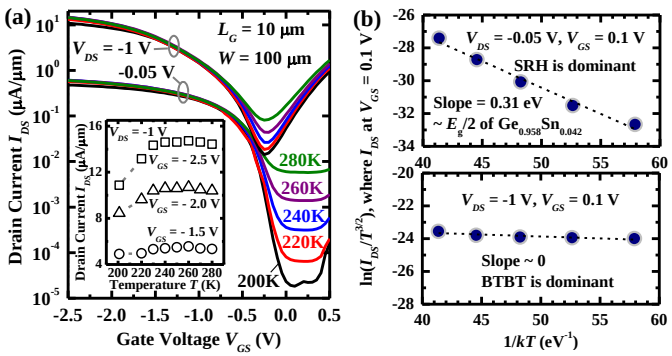

Fig. 11. (a) I_{DS}-V_{GS} characteristics measured at low temperatures ranging from 220 to 280 K. (b) Arrhenius plot of ln(I_{DS}/T3/2) versus 1/kT for V_{DS} = -0.05 V and -1 V

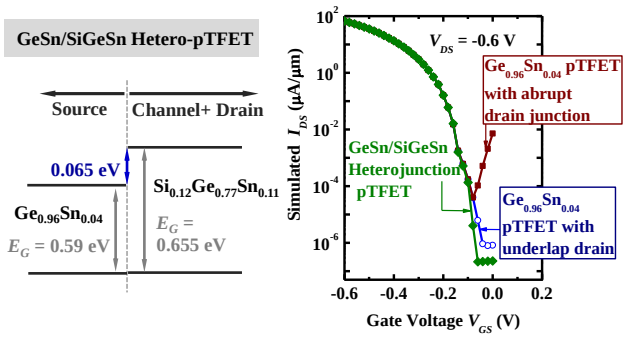

Fig. 12. The simulation results show that drain engineering with $GeSn_{0.04}/Si_{0.12}Ge_{0.77}Sn_{0.11}$ heterojunction or with underlap drain structure can achieve lower I_{off}.