Demonstration of High Electron Mobility in Germanium n-channel Junctionless FETs

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Abstract
We have demonstrated the high electron mobility in Ge n-channel junction-less FET for the first time, and discussed its electrical properties. The on/off ratio of ~10^5 was achieved by thinning the Ge thickness down to 15 nm. The field effect mobility in the first order estimated to be ~1000 cm^2/Vs. Then, a comparison of the value with the bulk mobilities of n-Si and n-Ge is made.

1. Introduction
Junction-less FETs (JL-FETs) are gaining much attention for solving the problem of sharp doping profile formation and for improving the short-channel effects. In fact, Si nanowire FETs with no pn junction have been reported [1]. Concerning the device performance, it is also claimed that JL-FETs show less sensitivity to the channel interface and have a better speed performance by making use of the bulk mobility. However, since the Si nanowire JL-FETs need to be fabricated on heavily doped SOI, a significant mobility enhancement in Si has not been obtained. Then, we have already demonstrated Ge p-channel JL-FETs based on its high bulk hole mobility [2]. Meanwhile, it should be noted that the electron mobility in bulk n-Ge is more interesting from the viewpoint of the fact that one order higher than that in n-Si in heavily doped region (N_d=10^{18}-10^{19} /cm^3) [3]. In this work, we demonstrate n-channel JL-FET fabricated on GeOI substrate for the first time.

2. Device Fabrication
A heavily-doped 90nm-thick n-type GeOI wafer with 100-nm-thick buried SiO_2 and intrinsic Si was used. The fabrication process and the device structure of JL-FET in this work is described in Fig. 1. First, the mesa type Ge islands were defined by wet-etching. Next, Ge islands were thinned down to 15-32 nm by a wet-etching process only for the channel region, and 80-nm-thick Ge remained for the source/drain (S/D) regions to make electrical contacts better. After cleaning with methanol and HCl, 20nm-thick Y_2O_3 was deposited onto the Ge islands by rf-sputtering, followed by annealing at 550°C in O_2 to passivate the surface defects. Prior to electrode formation, the sample was oxidized at low-temperature (400°C) to form the very thin GeO_x layer on S/D region, and then to weaken the Fermi-level pinning near the Ge valence band edge [4]. Finally, Al was deposited and patterned for S/D. Al was also deposited on the backside of Si as the back gate electrode. To subtract the parasitic resistance, four-point probe arrangement was prepared.

From secondary ion mass spectroscopy (SIMS) analysis, the average doping concentration in the present GeOI (20-30 nm-thick) wafer was around 2x10^{18} /cm^3, and Phosphorus was uniformly distributed in entire Ge film, while Arsenic was profiled, as shown in Fig. 2.

3. Results and Discussion
Fig. 3(a) shows transfer characteristics of Ge n-channel JL-FETs with various Ge thicknesses. The on/off ratio of ~10^5 was achieved by thinning the thickness of Ge, so that the majority carriers in the channel were fully depleted. The subthreshold characteristic is expected to be further im-

Fig. 1 (a) The process flow, (b) The schematic and (c) The microscopic image of Ge n-type JL-FET. The potential bars enable us to perform 4-probe measurement.

Fig. 2 Donor impurity (phosphorus and arsenic) SIMS profile of n-type GeOI substrate. The concentration of the other dopants is under the detection limit.
proved by fabricating double-gate or gate-all-around structure.

On the other hand, the output characteristics of the device with 15-nm-thick Ge channel is shown in Fig. 3(b). It should be noted that Ge/Al contacts at source and drain did not show the perfect ohmic characteristics in spite of the formation of pinning-relaxation layer. Therefore, we employed the four-probe measurement to estimate the channel mobility. The voltage drop through the Ge channel can be measured without worrying about the parasitic resistance at source and drain. In this manner, the field effect mobility of Ge n-channel JL-FETs was estimated, as shown in Fig. 4. It is noted that high electron mobility (~1000 cm²/Vs) achieved in 32-nm GeOI case. On the other hand, the mobility degradation with decreasing the Ge thickness was clearly observed. Though the further investigation is obviously needed to clarify its microscopic origin, it seems to be attributed to the crystallinity degradation of GeOI and/or the existence of coulomb scattering centers at Ge/SiO₂ interface [5].

4. Summary

We demonstrated the high electron mobility in Ge n-channel JL-FET for the first time. The highest value of field effect mobility and on/off ratio were ~1000 cm²/Vs and 10⁴, respectively. Although, the S/D contact formation is a big issue to consider carefully, the channel mobility of Ge n-channel JL-FET is much higher than the bulk mobility of n-Si which is the limitation of Si n-channel FET.

ACKNOWLEDGEMENTS

One of the authors (S. Kabuyanagi) is grateful to the SEUT fellowship program in the University of Tokyo for the financial support.

REFERENCES