

Floating-Gated Memory Based on Carbon Nanotube Field-Effect Transistors with Si Floating Dots

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Abstract

We have fabricated carbon nanotube field-effect transistor (CNTFET)-based memory devices with Si floating dots. The electrical measurements reveal that the devices have both large hysteresis and long-term retention. The results indicate that CNTFET-based memory with Si floating dots is one of the candidates to overcome the tradeoff between hysteresis width and retention time.

1. Introduction

Carbon nanotubes (CNTs) have attracted attention as a post-silicon material since they have semiconducting property and high mobility [1]. In particular, CNT field-effect transistors (CNTFETs), in which semiconducting single-walled CNTs (SWNTs) are used as channels, are expected to be applied as highly integrated CNT-based circuits and highly sensitive label-free sensors [2-5]. Recently, many advances in device application based on CNTFETs, such as nonvolatile memory [2, 5] or logic gates [4], have been achieved. In the memory based on CNTFETs, differently from conventional metal-oxide-semiconductor field-effect transistor (MOSFET) based memory device, the electric field from the gate electrode is concentrated in the SWNT channel surrounded by gate dielectrics in CNTFETs, indicating that a high electric field can be easily obtained around SWNTs at low gate voltages since SWNTs have a small diameter of ~1 nm.

Many types of memory devices based on CNTFETs have been reported [2, 4]. In general, memory devices have a tradeoff relationship between hysteresis width and retention time. The CNTFET-based memory with Au floating dots obtained short retention time. On the other hand, the CNTFET-based memory with HfO₂ charge storage layer obtained small hysteresis width.

In this study, we have fabricated nonvolatile memories based on CNTFETs with Si floating dots, as shown in Fig. 1(a), and have investigated the electrical characteristics. Since Si floating dots have a narrow energy gap and a good adhesive property, enhancement of hysteresis width and retention time in CNTFET-based memories will be expected. In this work, the electrical characteristics in the devices with the Si floating dots were compared with that of devices with HfO₂ charge storage layer or Au floating dots.

2. Experimental Procedure

The fabrication method of CNTFET-based memory shown in Fig. 1(a) was as follow: The CNTFETs were fabricated on SiO₂/Si substrates. First, 5 nm of cobalt catalysts were patterned by photolithography and electron-beam evaporation onto the substrate. The SWNTs were synthesized by thermal chemical vapor deposition (CVD) at 900 °C for 10 min, using C₂H₅OH as the source alcohol gas. Then the Ti/Pd (2 nm/30 nm) source and drain electrode were formed by photolithography and electron-beam evaporation. Subsequently, the Al₂O₃ film (3 nm), acting as a tunneling layer, was deposited by using atomic layer deposition (ALD). The Si floating dots were deposited using catalytic chemical vapor deposition (Cat-CVD). Figure 1(b) shows an atomic force microscope (AFM) image of Si dots. Then Al₂O₃ film (10 nm) was also formed as a blocking layer. Finally, a Ti/Pd top-gate electrode was patterned by photolithography and electron-beam evaporation. An optical image of CNTFET-based memory was Fig. 1(c).

3. Results & Discussion

Figure 2(a) shows transfer characteristics of the devices, which were measured by sweeping the top-gate bias between -5 and 5, -3 and 3, and -1 and 1 V. The counter clockwise hysteresis loops are attributed to the charging and discharging processes of holes in the devices. Owing to concentration of electric field, the large hysteresis was observed. Figure 2(b) shows average hysteresis-sweep width characteristics for devices with Si floating dots and devices with HfO₂ charge storage layer, indicating that the hysteresis width of devices with Si floating dots is larger than that of devices with HfO₂ charge storage layer.

Figure 3 shows band structures of the devices with Si floating dots and with HfO₂ charge-storage layer. The Si floating dots have a narrower energy gap than the HfO₂ charge-storage layer. Since the narrower energy gap of Si allows the charges to be more easily injected from CNTs, the devices with the Si floating dots have larger hysteresis than those with HfO₂ charge storage layer.

Figure 4 shows retention characteristics of the devices with the Si floating dots. The drain current was monitored at a read voltage of 0 V. The measurements were carried out after performing a write and erase operation by applying the pulse of ±5 V for 1 s. The on/off ratio of the drain current (10³ of on/off ratio) was retained over 600 s. For comparison, retention properties were investigated for a device

with Au dots. The result indicates that devices with the Si floating dots have longer-term retention characteristics than that with Au floating dots. Since dangling bonds in Si dots have good adhesive property, the charge leakages in the devices with Si floating dots were reduced.

4. Conclusions

The CNTFET-based memory devices with Si floating dots have been investigated. The hysteresis characteristics of the devices are larger than that of the devices with HfO₂ layer, and the retention characteristics of the devices with Si floating dots are superior to those of the devices with Au floating dots. Therefore, the Si floating dots will be useful to fabricate CNTFET-based memory devices with high performance.

Acknowledgements

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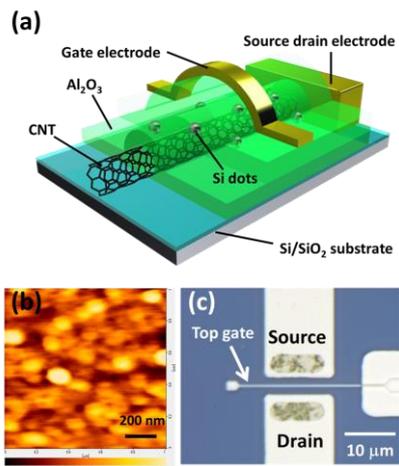


Fig.1. (a) Schematic image of CNTFET-based memory. (b) AFM image of Si floating dots. (c) Optical image of CNTFET-based memory.

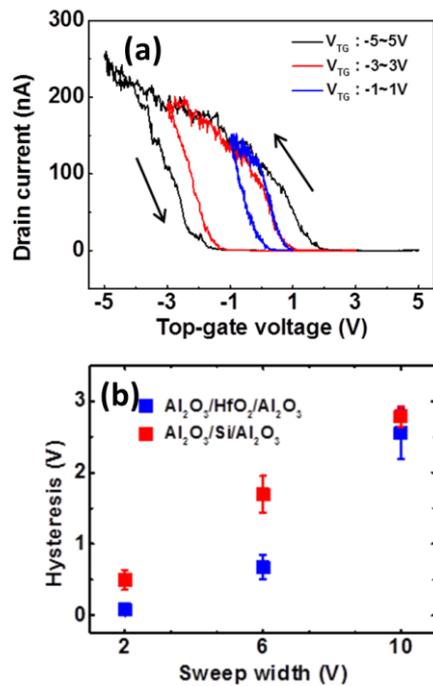


Fig.2. (a) Transfer characteristics of devices with Si floating dots. (b) Average hysteresis-sweep width characteristics for devices with Si floating dots and devices with HfO₂ charge storage layer

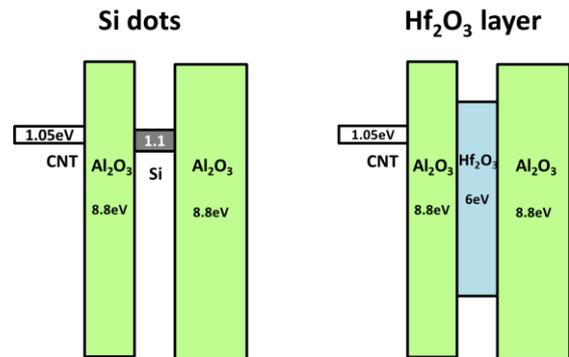


Fig.3. The band structures of devices with Si floating dots and devices with HfO₂ charge storage layer.

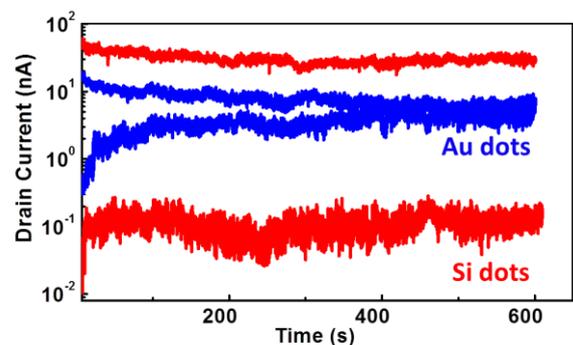


Fig.4. The retention characteristics of devices with Si floating dots and devices with Au floating dots.