1. Introduction

Graphene is expected to realize higher speed operation of FETs, because a very high carrier mobility in excess of 200,000 cm²V⁻¹s⁻¹ is experimentally reported [1]. However, since graphene has no band gap, it cannot be used as a switching device in logic circuits. So far, several methods have been proposed to open a band gap, such as graphene nanoribbon (GNR), graphene nanomesh and bilayer graphene (BLG) applied by a vertical electric field. Although those graphene nanomaterials have nonzero effective masses as a result of the band gap opening, Harada et al. [2] and Hosokawa et al. [3] reported that BLG and armchair-edged GNR (A-GNR) have the potential to surpass the speed of conventional Si and InP transistors. In this study, we intend to evaluate the power performance of A-GNRFETs, another important performance metric, by using an atomistic simulation. Furthermore, in terms of lower-power operation, nanowire (NW) MOSFETs are the leading candidate owing to their excellent gate electrostatics by employing gate-all-around (GAA) configurations. Hence, we also make a comparison between A-GNRFETs and NW-FETs consisting of Si and InAs NW channels.

2. Band Structures

First, we calculated the band structures of A-GNRs using a tight-binding (TB) approach [4]. We considered up to the third-nearest-neighbor interactions and overlaps to obtain more accurate dispersion relations in wide range of wave vectors as shown in Fig. 1(a), where \( \gamma_0 (s_0), \gamma_1 (s_1), \) and \( \gamma_2 (s_2) \) are the TB parameters for the nearest, second-nearest, and third-nearest-neighbor interactions (overlaps), respectively. Their values were taken from [4] as \( \gamma_0 = -2.97eV, \gamma_1 = -0.073eV, \gamma_2 = -0.33eV, \) and \( s_0 = 0.073, s_1 = 0.018, s_2 = 0.026. \) In addition, the onsite energy \( \epsilon_{sp} \) was given as -0.28eV. In this study, edge bond relaxation [5] was not taken into account. Figs. 1(b), (c), and (d) show the calculated band structures for \( N = 6, 9, \) and 12, respectively, where \( N \) is the number of carbon atoms in the width direction. As is well known [3,5], the band gap and the electron effective mass decrease with increasing the ribbon width.

Next, the band structures of Si NWs and InAs NWs were calculated using the \( sp^3d^5s^* \) TB model [6,7], as shown in Figs. 2(a) and (b), respectively. The upper panels of Fig. 2 show the atomic models used in the calculations for the two wire orientations of \(<100>\) and \(<110>,\) where surface atoms were passivated using an \( sp^3 \) hybridization scheme [6]. First, note that the present InAs NWs have band gaps of larger than 1eV, which allows us to neglect band-to-band tunneling leakage current at an OFF-state bias. For Si NWs, the \(<110>\) orientation has transport mass smaller than the bulk \( m_0 = 0.19 \) \( m_0, \) while the \(<100>\) orientation has the one slightly larger than \( m_0, \) which is because of the anisotropic and nonparabolic conduction band structure of Si [7,8]. On the other hand, both of the InAs NWs have significantly larger effective masses than that of the bulk \( m_0, \) 0.026\( m_0 [7,9]. \) This is due to the highly nonparabolic dispersion curves of the \( \Gamma \) valleys. In Fig. 3, we plotted the effective mass vs. band gap relationships for the A-GNRs and the NWs, showing that the A-GNRs exhibit larger effective masses than those of common III-V compounds at the same band gap [10]. Here, it shall be interesting to note that the InAs NWs still satisfy the linear relationship governing III-V compounds. Therefore, the InAs NWs exhibit the smaller effective masses than those of the A-GNRs under the same band gap.

3. Electrical Characteristics

We employed a top-of-the-barrier (ToB)-FET model [11] to evaluate the electrical characteristics as shown in Fig. 4, where any scattering mechanisms and off-state tunneling leakage currents are neglected. Fig. 5 shows the \( I_D - V_G \) characteristics computed for (a) A-GNRFETs and (b) Si and InAs NWFETs with \( T_{ox} = 0.5 \) nm, where the drain currents are normalized by the width of the single gate in (a) and by the perimeter of NWs in (b), to make a fair comparison under the same gate electrostatics. It is found that the A-GNRFETs exhibit sufficiently high drain current even for \( V_G < 0.6V. \) In Fig. 5 (b), the drain current of the InAs NWFETs becomes comparable to or even smaller than that of the Si NWFETs, which is due to the influence of a quantum capacitance [7]. Next, Fig. 6 shows the intrinsic device delays as a function of gate voltage, where the channel length \( (L_{ch}) \) is taken as 12nm. It is found that the A-GNRFETs and the InAs NWFETs have the intrinsic delays below 0.1ps for \( V_G < 0.6V, \) which meets the ITRS requirements for 2024. Finally, Fig. 7 shows the power delay product (PDP) densities as a function of drain current. Here, it is worth noting that the A-GNRFETs indicate a lower switching power density than the InAs NWFETs, comparing at the same \( I_D. \) This means that the A-GNRFETs need a smaller sheet charge density for switching a device, owing to its atomically-thin channel structure. We have confirmed that the above conclusion regarding the PDP density is true for thicker \( T_{ox} \) devices.
4. Conclusions

Under the ballistic transport regime, A-GNRFETs were shown to have the potential to outperform Si and InAs NWFETs in terms of lower-power operation.

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Fig. 1 (a) Atomic model of A-GNR, and band structures computed for \( N = 3 \) (b), 6, (c) 9, and (d) 12. \( E = 0 \) corresponds to the Fermi level.

Fig. 2 Band structures computed for (a) InAs NWs and (b) Si NWs with \(<100>-\text{InAs NW}\) and \(<110>-\text{InAs NW}\) orientations, where the wire cross section is about \( 3 \times 3 \text{ nm}^2 \) for all NWs.

Fig. 3 Effective mass vs. band gap relationships for A-GNRs and NWs. The solid circles are for common III-V compounds, which are fitted by the dashed line. The solid triangles indicate the electron conductivity mass of Si and Ge.

Fig. 4 Schematic diagram of the simulated A-GNRFET and GAA-NWFET. We employed ToB-FET model. The gate insulator is assumed to be SiO\(_2\) with a thickness of 0.5 nm.

Fig. 5 Ballistic \( I_D-V_G \) characteristics of (a) A-GNRFETs and (b) Si and InAs NWFETs with \(<100>-\text{Si NW}\) and \(<110>-\text{InAs NW}\) orientations. \( T_{\text{ox}}=0.5 \text{ nm}, \ V_D=0.4 \text{ V}, \) and \( I_{\text{OFF}}=0.01 \mu\text{A}/\mu\text{m}. \ T=300 \text{ K}. \) In (b), the vertical axis denotes drain current density normalized by the perimeter of NWs.

Fig. 6 Intrinsic device delays computed as a function of gate voltage, where (a) A-GNRFETs and (b) Si and InAs NWFETs. The simulation conditions are the same as in Fig. 5. \( L_{\text{ch}}=12 \text{ nm}. \)

Fig. 7 PDP densities computed as a function of drain current, where (a) A-GNRFETs and (b) Si and InAs NWFETs. The simulation conditions are the same as in Fig. 5. The vertical axis denotes the PDP density divided by the in-plane device area.

References