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Ultra-low Damage Fabrication of Graphene Nanoribbons by Neutral Beam Etching

Takeru Okada[1], Ching-Yuan Su[2], Chi-Hsien Huang[2], Kouki Igarashi[1], Akira Wada[1], Lain-Jong Li[3], Kuan-I Ho[2], Pei-Wen Li[4], Inn-Hao Chen[4], Chao-Sung Lai[2†], and Seiji Samukawa[1,5⊥]

[1]Institute of Fluid Science, Tohoku Univ., 2-1-1 Katahira, Aoba-ku, Sendai, Japan

[2]Department of Electronic Engineering, Chang Gung University, 259 Wen-Hwa 1st Road, Kwei-Shan Tao-Yuan, 333

[3]Institute of Atomic and Molecular Sciences, Academia Sinica, Taiwan, Taipei 10617

[4]Department of Electrical Engineering, National Central University, Tao-Yuan 320, Taiwan

[5]WPI-Advanced Institute for Materials Research, Tohoku Univ., 2-1-1 Katahira, Aoba-ku, Sendai, Japan

E-mail: †cslai@mail.cgu.edu.tw, ⊥samukawa@ifs.tohoku.ac.jp,

Abstract

Ultra-low-edge-defect graphene nanoribbons (GNRs) are successfully fabricated by subjecting large scale CVD graphene to a combination of electron beam lithography and oxygen neutral beam etching. Atomic force microscopy (AFM) images clearly show the morphology of the GNRs and Raman spectroscopy shows they have extremely low I_D/I_G ratio. A bottom-gate field-effect transistor with an array of the GNRs is found to have a high on/off ratio (~10^4) and high carrier mobility (~200 $cm^2\ V^{-1}\ s^{-1}$) even at room temperature.

1. Introduction

Since the first report in 2004 [1], graphene has attracted much attention and research interest because of its unique characteristics. Graphene is certainly a promising material for advanced electronic devices [2]. However, the fact that it is a semimetal with zero bandgap and has a high conductivity even at the charge neutrality point means its potential application in field-effect transistors (FETs) operating at room temperature is limited [3]. One useful way to overcome this problem is the fabrication of Graphene nanoribbons (GNRs). With their quasi-one-dimensional graphene nanostructure, GNRs have an effective bandgap (E_g) because of the lateral confinement of charge carriers and circumvent some of the problems encountered by the gapless band structure of 2D graphene [4]. Several approaches have been used to fabricate or synthesize GNRs. Among existing approaches, top-down lithography; i.e., lithographic patterning followed by top-down O_2 plasma etching, is very attractive for fabricating well-arranged GNRs required for very-large-scale integration. However, conventional O_2 plasma etching unavoidably produces plenty of defects on the edges of GNRs. Therefore, it has proven to be difficult to obtain a large E_g and sufficient mobility for room-temperature operation of GNR-based FETs using wide GNRs (>10 nm).

In this study, we report GNRs lithographically patterned by electron beam lithography (EBL) followed by O_2 neutral beam etching (NBE). Compared with conventional O_2 plasma etching, NBE is an advanced top-down etching technique that imposes low defects and produces high quality GNRs. The morphology of the GNRs was observed by atomic force microscopy (AFM). The high quality of the GNRs with low defects at the edges was confirmed by Raman spectroscopy. We also demonstrated a back gate transistor with a GNR array, which showed a high carrier mobility at room temperature.

2. Experiment

The GNR sample was prepared by growing a large-sized monolayer graphene film on high purity copper foil by CVD in a tubular quartz furnace [5]. The as-grown graphene was transferred from the foil to a thermally grown SiO_2 (300 nm thick) substrate on a heavily p-doped Si substrate (SiO_2/Si). The GNRs were prepared by EBL patterning followed by O_2 NBE with the following conditions: a chamber pressure of 0.7 mTorr, an RF power of 250 W, and an irradiation time of 3.5 min. A film of the negative tone resist hydrogen silsesquioxane (HSQ), with a thickness of around 150 nm, was spin-coated onto the graphene/SiO_2/Si. The unmasked graphene area was etched by O_2 NBE. After removing the HSQ by using diluted hydrofluoric acid, we obtained GNRs on the SiO_2/Si substrate. Four GNR arrays with widths of 30, 50, 70, and 100 nm were fabricated, and their length was around 8 µm. In order to ensure a sufficient Raman signal for the analysis, A total of 10–15 nanoribbons of the same width were fabricated in an array spanning 2-3 µm.

After GNRs fabrication using EBL patterning followed by O_2 NBE, we also fabricated back gate FETs with GNR array (width: 70 nm; nanoribbon number: 10) as channel to evaluate the electric property of GNRs. The GNR array was covered with a Cu grid (as a shadow mask), and Cr/Au (2 nm/60 nm) source and drain electrodes were subsequently deposited on the GNR array by a thermal evaporator to form the FET. The FET channel was 5 µm in length, and the width of the source and drain electrodes was 12 µm. All electrical measurements were performed under ambient conditions using a Keithley-4200 semiconductor analyzer.

3. Results and Discussion

Figure 1 shows AFM images of the fabricated GNRs after the NBE process. They show the unmasked region was clearly etched away by NBE. It was found that the GNR array was uniformly fabricated on a large scale [6]. Figure 2 shows the ratio of intensities of the D- and G-bands, denoted as I_D and I_G respectively. The ratio indicates the defect level at the GNR edge. The I_D/I_G ratio increases as the GNR width decreases; however, the ratio is impressively lower than that of the GNRs fabricated by conventional O_2 plasma etching as shown in reference in Fig 2. This is due to the reduction of UV irradiation damage. The irradiation of UV photons is isotropic, hence UV can penetrate into the resist and reach the GNR from the edge. Therefore, in the case of conventional plasma etching, the C-C bonds at the edge of the GNR are destroyed to form a wide range of defects observed as high I_D/I_G from Raman spectrum. In contrast, the UV photons are almost eliminated in a NBE system. Thus only a narrow range of defects, contributing to small I_D/I_G, is induced owing to the C-C bond breakage at the edge resulting from NB bombardment [6]. In addition, the ratio is comparable to that of GNRs prepared by unzipping carbon nanotubes which is shown as diamond symbol in the Fig 2.

To evaluate the electrical characteristics of the GNRs fabricated by NBE, we fabricated a back gate field effect transistor (FET) with a GNR array of 10 nanoribbons (width: 70 nm). The mobility (μ) was extracted on the

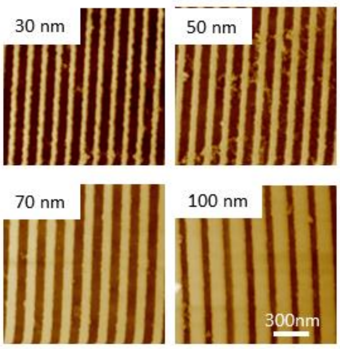

Figure 1. AFM images of GNRs.

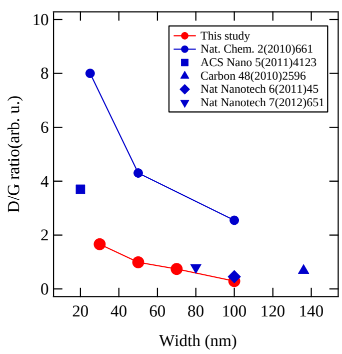

Figure 2. Ratio of the integrated intensities of the D- and G-bands (I_D/I_G) as a function of the GNR width. Results are shown for GNRs prepared by our method and other approaches.

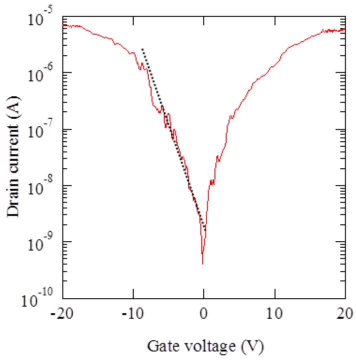

Figure 3 Drain current vs. gate voltage (I_d vs. V_g) of the FET with a GNR array of 10 GNRs (width: 70 nm). (V_{sd} = 0.5 V)

basis of the slope ΔI/ΔV as indicated by the dashed line fitted to the linear regime in Fig. 3[6]. The effective mobility was more than 200 [$cm^2\ V^{-1}\ s^{-1}$]. This is high for a CVD-grown GNR since CVD-grown graphene inevitably contains grain boundaries in the channel region, especially in a long channel (5 μm in this study). Furthermore, we observed high I_{on}/I_{off} current ratio around 10^4 at room temperature, which is much higher than other reported results. This large I_{on}/I_{off} current ratio is considered to be contributed from transport gap, which may result from a long-channel effect [7].

3. Conclusion

In conclusion, we have demonstrated that low edge defects were incurred in GNR arrays fabricated by patterning CVD-grown graphene by EBL followed by O_2 NBE. Raman analysis showed that ultra-low-damage GNR arrays can be fabricated. This is because a NB system can provide low energy and well-controlled NBs without UV irradiation. To evaluate the electrical characteristics of the GNRs we fabricated a back gate FET with an array of 70 nm wide GNRs; it was shown to have a high mobility of ~200 [$cm^2\ V^{-1}\ s^{-1}$] and a high I_{on}/I_{off} ratio (~10^4). From these results we believe this method should prove useful for fabricating high performance GNR-based electronic devices for very-large-scale integrated circuits.

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