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Experimental Study on SET/RESET Conditions for Graphene ReRAM

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1. Introduction

Due to the outstanding electrical and thermal properties, graphene has attracted great attentions as a new material for future nanoscale electron devices. Many studies have been reported on applications of graphene in FETs [1], interconnects [2], and diodes [3]. We have reported that two-terminal graphene device operates as resistive random access memory (ReRAM) [4]. Although there are some reports on memory effect in graphene [5, 6], bias conditions for SET/RESET have not been fully studied. In this study, we investigated the bias conditions to observe ReRAM effects in graphene. It is found that, for the SET operation, high drain or high gate voltage is necessary whereas electrical current can be quite small.

2. Experimental

Two- or four-terminal (2-T or 4-T) graphene ReRAMs shown in Fig. 1 were utilized. The four terminals are referred as T_1 to T_4. The voltage and current between two terminals, for example T_1/T_4 as the biased/reference nodes, are expressed as V_{14} and I_{14}. All the electrical measurements were performed in the vacuum chamber at the pressure of lower than 10^{-2} Pa.

3. Results and Discussion

A. Location of ReRAM Point in 4-T Devices

It is sometimes speculated that the ReRAM effect may originate from graphene/metal interface. In order to clarify the location of ReRAM effect, we utilized 4-T devices. The forming operation between T_1 and T_4 (T_1-T_4 forming) is shown in Fig. 2. The resistive changes in three areas (T_1-T_2, T_2-T_3, T_3-T_4) of 4-T devices after T_1-T_4 forming/SET operations are shown in Fig. 3a. Although the bias is applied only to T_1, only the resistance of T_2-T_3 area is changed. I_D-V_G of T_1-T_2 area after T_1-T_4 forming/SET is shown in Fig. 3b, indicating that the characteristics of T_1-T_2 area are independent of T_1-T_4 operations. These results clearly demonstrate that the graphene/metal interface is not the origin of the ReRAM effect.

B. SET/RESET Conditions for Two Series ReRAM Points

A system containing two ReRAM points is built by two forming processes (Fig. 4a). The first ReRAM operation point was formed in T_2-T_3 area by T_1-T_3 forming. The second one was formed in T_1-T_2 area by T_1-T_2 forming.

SET operation is performed by applying V_{13} when both the operation points are in high resistance state (HRS) as shown in Fig. 4b, leading to the successful SET operations for both the ReRAM points. On the contrary, in RESET operation, where V_{13} is applied to the system containing two low resistance state (LRS) points, the higher resistance LRS point switched to HRS and the lower resistance LRS point did not (Fig. 4c). This implies that only one ReRAM point exists between the nearest two terminals. Once ReRAM point is constructed by forming operation, the resistance of ReRAM point is higher than other areas. Thus, another ReRAM point will not be newly generated.

C. Interference between Two ReRAM Points

To investigate the interference between two ReRAM points, the effect of electrical readout on the adjacent device is studied. Figure 5a shows that I_{12}-V_{12} measurement (V_{12} < 1.5 V) throws no impact on the T_2-T_3 ReRAM point.

On the other hand, I_D-V_G measurement of the T_1-T_2 ReRAM point influences the resistance state of T_2-T_3 ReRAM point (Fig. 5b). The resistance of T_2-T_3 area was decreased by approximately 10^6 in magnitude; SET operation was performed by I_D-V_G measurement in the adjacent device. To analyze its origin, V_G was applied to 2-T ReRAM in HRS with $V_S = V_D = 0$ V as shown in Fig. 6. During the measurement, I_S, I_D, and I_G are monitored, showing that SET operation is possible by V_G with extremely low I_D. Another measurement confirms that the absolute value of V_G needs to be higher than the specific value, whereas the polarity of V_G is not important.

To further examine the SET operation, I_D and V_D necessary to switch from HRS to LRS are obtained. Figure 7a shows the definition of SET voltage (V_{SET}) and current (I_{SET}). The relationships between R_{HRS} and V_{SET} as well as R_{HRS} and I_{SET} are shown in Fig. 7b, suggesting that the SET operation is driven by the voltage, or potential difference, in ReRAM device.

The application of either V_D or V_G enables SET operation. However, RESET operation can be achieved only by V_D. It is prospected that SET and RESET operations have different mechanisms for the resistance change.

D. Evaluation of SET operation by Gate Voltage

Figure 8a shows the resistance distribution after the SET operation by V_G. Although SET operation occurs with *floating source/drain*, resistance distribution is much wider and the retention characteristics are worse than those obtained with *grounded source/drain* (Fig. 8b).

Figure 9a shows the time dependence of I_D during three operations with V_D of 1 V. The left, middle, right figures correspond to read (HRS), SET, read (LRS) operations. As shown in the middle figure, until the time when the application of V_G was finished, the I_D is kept at the same value. This result suggests that SET operation occurred at the transient of V_G down to 0 V.

Another experiment also supports this idea. When V_G is dropped with a small step of 1 V after the same SET operation as the one shown in Fig. 6, SET operation fails. This situation is shown in Fig. 9b. This result means that for SET operation abruptness of the V_G change is necessary.

4. Conclusions

The bias conditions for SET/RESET operation in graphene ReRAM have been studied. It is shown that ReRAM effects occur in a limited part of graphene channel and that ReRAM effect is not due to the graphene/metal interface. It is suggested that the SET operation is driven by the voltage, or potential difference, in ReRAM device. In addition, it is confirmed that SET operation is possible by V_G with extremely low I_D. SET operation occurred at the transient of V_G down to 0 V.

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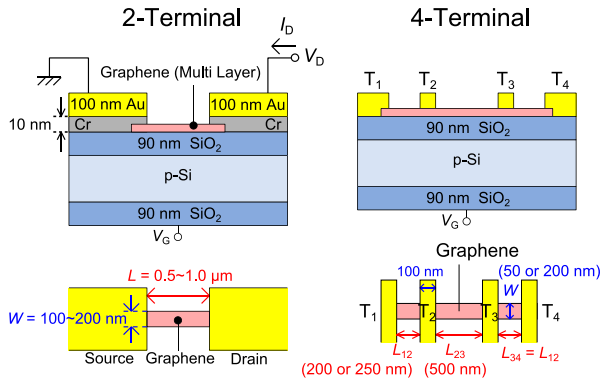


Fig.1: Schematic of device structure. In 4-terminal (4-T) device, four independent electrodes are defined as T_1 to T_4.

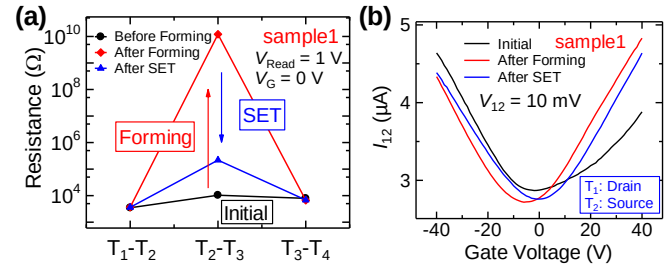


Fig.3: **(a)** Resistance change of each area after T_1-T_4 forming/SET operations. Only T_2-T_3 area operates as a memory and other areas keep original characteristics. **(b)** I_D-V_G characteristics of T_1-T_2 area. It is shown that switching of T_2-T_3 area has no effect on other areas.

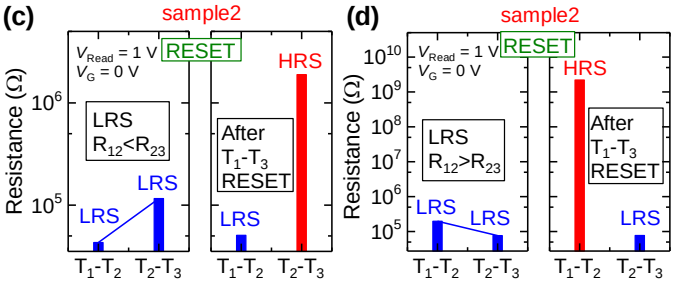


Fig.4: **(c) (d)** Resistive change through T_1-T_3 RESET operation. The area with higher R_{LRS} changes to HRS after T_1-T_3 RESET.

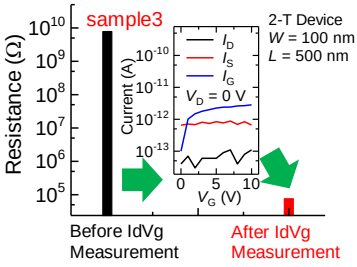


Fig.6: SET operation with V_G. During the SET operation, V_D is set to 0 V and extremely small drain current is observed, indicating that large current is not necessary for SET operation.

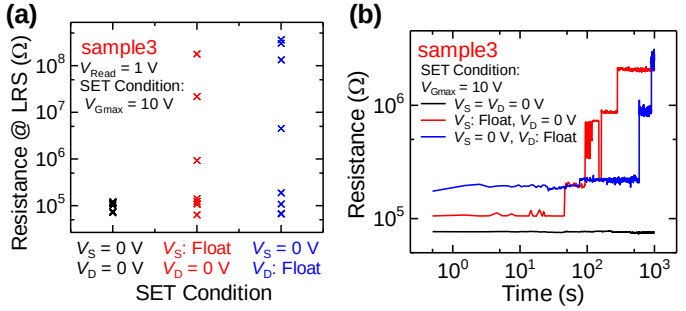
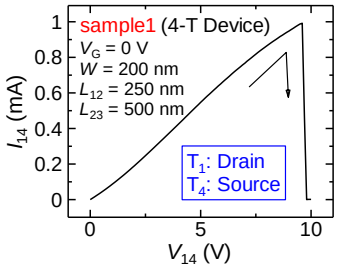


Fig.8: **(a)** Resistance distribution obtained by SET operation with V_G. Although switching occurs even under the condition of *floating source/drain*, the condition of *grounded source/drain* provides best LRS condition. **(b)** Retention characteristics of R_{LRS} obtained by SET operation with V_G. It is shown that the condition of *grounded source/drain* provides most stable resistance.



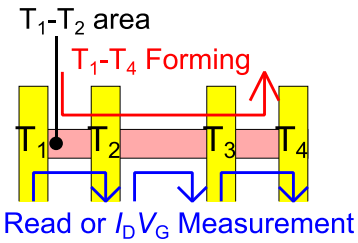


Fig.2: Forming characteristics of 4-terminal device. T_1 and T_4 are used as the drain and source, respectively. V_{14} and I_{14} are defined as the voltage of T_1 with respect to T_4 and the current flows from T_1 to T_4.

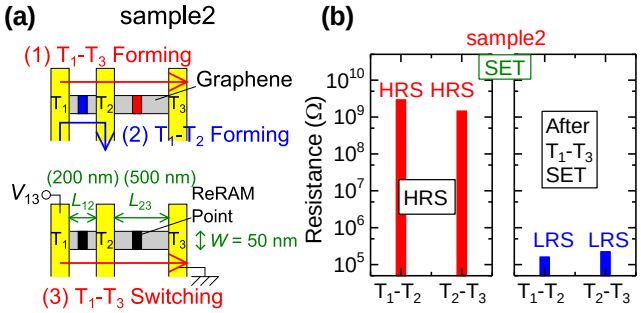


Fig.4: **(a)** Schematic of two ReRAM points connected in series. After ReRAM point of T_2-T_3 area is formed by T_1-T_3 forming, T_1-T_2 forming is performed as second forming. **(b)** Resistive change through T_1-T_3 SET operation. Both HRS points are switched to LRS.

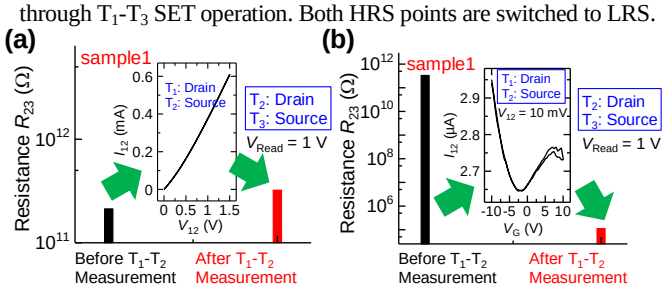


Fig.5: **(a)** Resistance change of T_2-T_3 area with I_{12}-V_{12} measurement. It is shown that I_{12}-V_{12} measurement has no effect on T_2-T_3 area. **(b)** Resistance change of T_2-T_3 area with I_D-V_G measurement on T_1-T_2 area. After the measurement, resistance of T_2-T_3 area decreased, indicating that I_D-V_G measurement on T_1-T_2 area has SET effect on T_2-T_3 area.

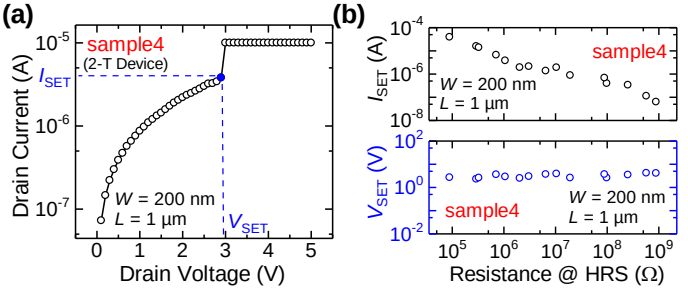


Fig.7: **(a)** Definition of SET voltage V_{SET} and current I_{SET}. **(b)** V_{SET} and I_{SET} as a function of R_{HRS}. Compared to the resistance and current range, the voltage range is extremely limited, indicating that the qualification of SET operation is related to potential difference in ReRAM device.

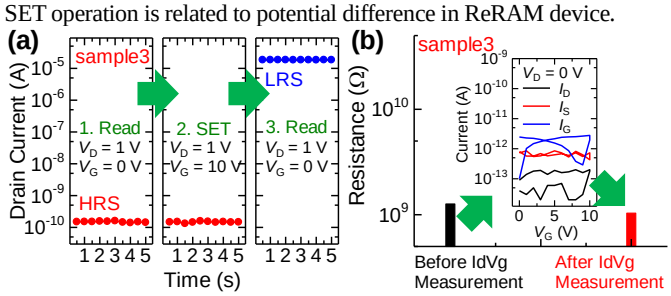


Fig.9: **(a)** SET operation under the condition of V_D = 1 V. It is shown that R_{HRS} is kept during the SET operation. **(b)** SET operation with double sweep of V_G. Although high enough voltage and current are supplied, the resistance is kept as HRS, indicating that SET operation occurs when V_G is released.