Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp674-675

Carbon Nano-materials as VLSI Interconnects

John Robertson, H Sugime, S Esconjauregui, G Zhong, C Zhang, R Xie, B Chen

[1] Engineering Dept, Cambridge University, Cambridge CB2 1PZ, UK
Phone: +44-1223-748331 E-mail: jr@eng.cam.ac.uk

Abstract

Carbon nanotubes and graphene have great potential as interconnects in VLSI integrated circuits, due to their high current carrying capacity, and for CNTs, their ability to form high aspect ratio structures. We review their growth and integration by chemical vapor deposition.

1. Introduction

The continued scaling of VLSI device dimensions means that the current densities carried by interconnects will soon exceed the limits of copper, ~6.10^6 A/cm^2 [1,2]. Only carbon, either carbon nanotubes (CNTs) or graphene can carry a higher density**.** This leads to the concept of the all carbon interconnect, with CNTs as the vertical vias and either CNTs or graphene as the horizontal wires.

Scaling is also leading to 3 dimensional integration which requires interconnects between layers – through – silicon vias (TSVs). CNTs have opportunities here because of the difficulty of depositing the standard metals in high aspect ratio holes for TSVs.

Both applications require extremely high control of the chemical vapor deposition process used to fabricate the CNTs or graphene, and developing integration methods for back end of line temperatures (400C).

2. Vias

The objectives for vias is to grow CNTs by chemical vapor deposition (CVD) with the highest density possible, ideally $3x10^{13}cm^{-2}$, at a temperature close to 400C (back end of line), and to integrate them into a suitable process flow, with low contact resistances at both top and bottom contacts [1-3].

The ability to grow highly dense CNT forests depends on our ability to deposit growth catalysts with that density (Fig 1). We have developed five methods to do this, but it must be done on a conductive substrate. The catalyst nanoparticles are made by de-wetting. There are two difficulties, 1) that metallic support layers have high surface energies, which does not favor de-wetting, 2) one must avoid oxidation of the support layer in the process conditions (not easy).

First, we developed a cyclic catalyst deposition method to increase catalyst density [4] (Fig 2). This works well on Al_2O_3, and in principle should work on other substrates.

Second, we reduce the catalyst particle diameter, and so increase the area density, by stopping side-effects like catalyst diffusion [5].

Third, we can use techniques like catalyst immobilisation by plasma processing [6,7]. Many of these methods work best on insulating substrates, and need careful updating for metallic substrates. The MIRAI work is generally on conductive Ti/TiN substrates [1].

Fourth, we deposit catalyst on metallic substrates but use ultrathin Al_2O_3 layers to immobilize the catalyst [8] (Fig 3). Fifth, we can grow from a Fe-Ti-Fe multilayer catalyst, the upper Fe does the growth, the lower Fe acts to stop inward diffusion of the upper Fe [9].

Sixth, we have developed an unusual Co-Mo catalyst for low temperature growth, which works on Ti support layers. It gives unusually high CNT area densities. It has a mass density of 1.5 gm/cm^3 (Fig 4), one of highest yet [10,11]. Throughout these methods, area density is measured by weight gain in growth (Fig 5) [12]. Electrical data will be given.

3. TSVs

The stage of CNTs for TSVs is at a low state of development. Xie et al [13] recently demonstrated growth of CNTs in vias for TSVs (Fig 6).

4. CNTs for Horizontal Interconnects

Dijon et al [14] have developed a novel method for making horizontal interconnects. This involves growing patterned vertical CNT forests, and then flipping them into a horizontal position by liquid forces. A difficult part is aiming the CNT mat properly at the receiving electrode.

5. Graphene for Horizontal Interconnects

Graphene being a layered material is often considered for horizontal interconnects. Multi-layer graphene is OK. Again this should be grown in-situ by CVD. The problem is to do this at a sufficiently low temperature, not 850-1000C. Weatherup [15] recently showed how to lower growth temperatures to 450-600C by using Ni as catalyst.

Another way is to use solid-state conversion. Deposit C by PECVD as diamond-like carbon. Deposit Ni on top, then heat so the C diffuses though the Ni to form graphene on top [16]. The problem is that Ni grain boundaries make it non-uniform [17]. To avoid this, include an ultra-thin diffusion barrier to equalize diffusion across the layer. CNT growth on graphene is also needed [18].

References

1. Y Awano, et al, Proc IEEE **98** 2015 (2010)
2. J Robertson et al JJAP **51** 01AH01 (2012)
3. J Dijon, et al, IEDM (2010) p32.6
4. S Esconjauregui et al, ACS Nano 4 7431 (2010)
5. G Zhong, et al, ACS Nano 6 2893 (2010)
6. Y Yamazaki, APX 3 5502 (2010)

7. C Zhang, et al, Carbon 53 339 (2013)
8. S Esconjauegui et al, APL 102 113109 (2013)
9. G Zhong et al, Carbon (2013) submitted
10. H Sugime, et al, APL (2013) accepted
11. A Kawabata, JJAP 52 04CB06 (2013); SSDM (2012)
12. S Esconjauregui, JAP 113 144309 (2013)
13. R Xie, Nanotechnology 24 125603 (2012)
14. J Dijon, et al, Carbon 60 139 (2013)
15. R Weatherup, ACS Nano 6 9996 (2013)
16. Z Sun, Nature 468 549 (2010)
17. R Weatherup, et al, unpublished
18. R Rao et al, Sci Reports 3 891 (2013)

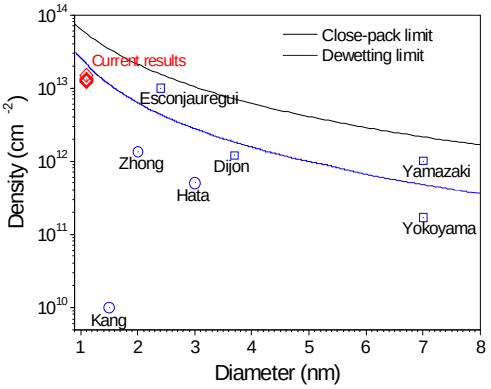

Fig. 1 CNT area density achievable by different techniques compared to close packed limit.

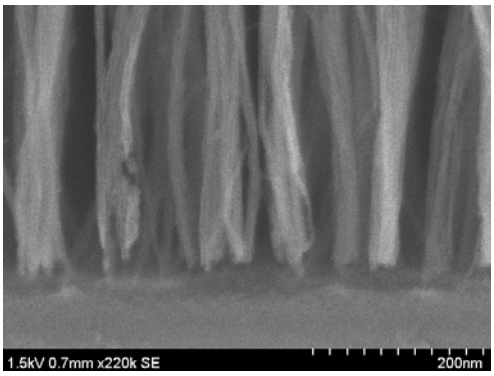

Fig. 2. High magnification SEM image of CNT forest grown by cyclic catalyst method [4].

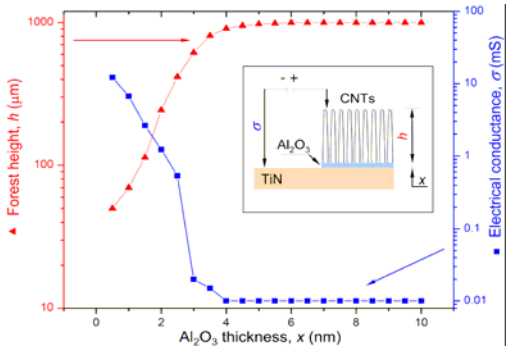

Fig. 3. Forest height and conductance of CNTs grown on ultra-thin Al2O3 on metal [8].

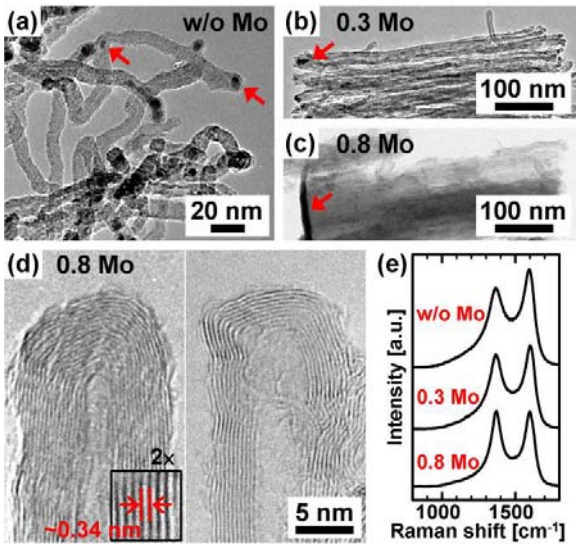

Fig. 4. TEM and SEM images of nanocarbon grown by Co-Mo catalyst at low temperature, with mass density if 1.5 g/cm3 [10].

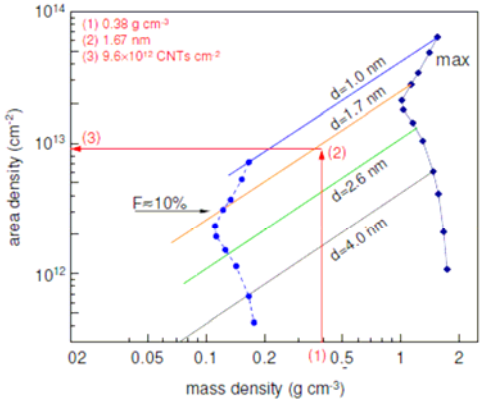

Fig. 5. Derivation of area density from measured mass density, if the average CNT diameter is known [12].

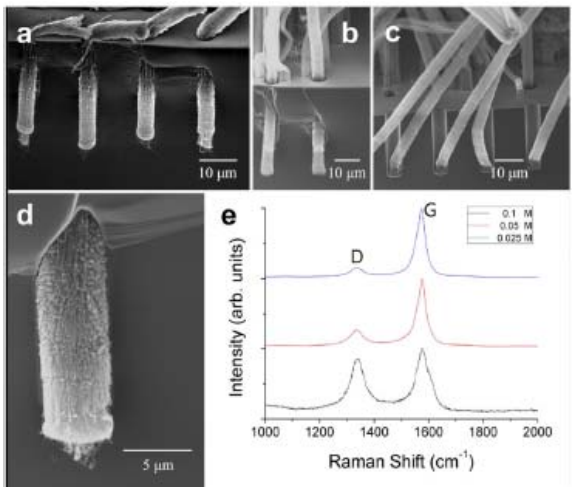

Fig. 6. Example of multiwall CNT grown in through-silicon-via using Fe as catalyst [13].