Reducing Carrier Density Pinning at Graphene/Metal Interfaces Using Multi-layer Graphene

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Abstract

In graphene field effect transistors (FETs), as the channel length becomes shorter, the apparent field effect mobility gets smaller. This is due to the carrier injection from metal electrodes (source and drain) to graphene, which makes the carrier density at the interface insensitive to the gate voltage. This carrier density pinning at the interface is unfavorable for graphene applications to electronics. Here, we show that insertion of multilayer graphene between graphene and metal electrodes improves the apparent mobility of short graphene FETs.

1. Introduction

Due to high mobility and atomic thickness, graphene is a promising candidate for the next-generation electronics material. Considerable effort has been devoted to achieve much higher mobility in graphene films. On the other hand, little attention has been paid to the effect of making contact between graphene and metals, which is indispensable for graphene electronic devices; Density functional theory has shown that metal contacts not only shift the Fermi level with respect to the Dirac point due to the difference in work function and carriers are injected to graphene. The change in the carrier density \( n \) extends by \( L_E \) from the interfaces as shown in Fig. 2(a) \((V_g = 0)\). For non-zero gate voltages, near the interface, the gate-induced carriers are compensated by carriers injected from the metal electrode, leading to the carrier density pinning at the interface. The resulting modulation of the conductance as a function of the gate voltage becomes smaller with shorter channel length, resulting in smaller \( \mu_{FE} \) [Fig. 2(b)]. The decrease of \( \mu_{FE} \) is remarkable for \( L < 2L_E \).

This carrier density pinning and resulting decrease of the field effect mobility is undesirable for the application of graphene to nanoelectronic devices, and should be lifted. One of the solutions for lessening the carrier density pinning would be to insert another material between the metal electrode and graphene. The inserted material should have a work function close to that of graphene and the contact resistance should not increase much by the insertion. For this purpose we choose multilayer graphene (MLG). In this paper, we report our method to insert MLG into the metal/graphene interface and electron transport in metal/graphene/metal structure with and without MLG-interfacial layer.

2. Sample Fabrication

For controlling the thickness and position of MLG, MLG is directly synthesized on graphene by using the methods reported in Refs. 4-7. First, by using e-beam lithography and liftoff, amorphous carbon (8 nm) followed by Ni (30 nm) is deposited on several places for electrode connection on single layer graphene, which is mechanically exfoliated from kish graphite. The substrate is then annealed at 750 degree in \( \text{H}_2 \) (2\%)/\( \text{Ar} \) atmosphere in a tube furnace for 15 min. After natural cooling, Ni layer is etched away using \( \text{FeCl}_3 \). After these procedures, the amorphous carbon turns into MLG. The Raman spectra of amorphous carbon and obtained MLG are shown in Fig. 3. Large G (~1650 cm\(^{-1}\)) and 2D (~2700 cm\(^{-1}\)) bands confirm the formation of MLG. Then metal electrodes (Pd/Au) are placed on top of the MLG using conventional e-beam lithography and liftoff. For comparison, graphene channel without MLG-interfacial layer with the same channel length is formed in the same graphene film, as shown in Fig. 4(a).
3. Transport Measurement

Figure 4(b) shows the gate-voltage dependence of resistance ($R-V_g$) in graphene channels ($L = 1 \mu m$) with and without the MLG-interfacial layer. The highly-doped Si substrate was used as the back gate. Note that $R-V_g$ curves should be parallel to each other with difference corresponding to the increase of contact resistance due to the interfacial layer, if the field effect mobility of graphene is the same for both samples. Thus, the observed larger slope in the graphene channel with MLG-interfacial layer in Fig. 4(b) confirms the reduction of the carrier density pinning and improvement of the field-effect mobility.

4. Summary

We have confirmed the reduction of the carrier density pinning at metal/graphene interface by inserting MLG-interfacial layer. Further study is needed to adjust the thickness and quality of MLG.

References