Standard CMOS Based One-Time Programmable Switches with Gate-Induced Permanent Source-Drain Path

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Abstract

Three-terminal one-time programmable switches using standard CMOS transistors are demonstrated. By gate-controlled programming, permanent conductive path is formed between the source and drain because of local breakdown in the PN junctions. Since different terminals are used between in programming and in reading, the proposed switch makes it easy to design the peripheral circuit. This method is applicable to standard CMOS devices and does not require any special manufacturing processes, which enables to realize the low-cost LSI with one-time programmable switches.

1. Introduction

Increase in LSI manufacturing cost has become a big problem. Therefore low-cost nonvolatile memories have been studied, but in general, the chip cost substantially increases when nonvolatile memories are embedded in the LSI because of the additional fabrication processes. For this reason, nonvolatile memories using standard CMOS transistors have been studied [1-4]. In particular, one-time programmable switch using a gate-ox-based anti-fuse has been reported, in which the source, drain and substrate are connected to the common terminal and current path is formed between the terminal and the gate using the breakdown of the gate dielectric [2-4]. The conventional anti-fuse, however, requires complex layout because of its singular current path, and furthermore it makes the peripheral circuits complicated because the same terminals are used for program and read operations.

Here we report novel one-time programming method to form permanent conductive path between the source and drain (S/D) in a standard CMOS transistor. The switch can be used as the anti-fuse. While the current path is formed between the S/D, programming is controlled by gate voltage, resulting in simple peripheral circuits. In addition, this method requires no special manufacturing processes, therefore the LSI in which one-time programmable switches are embedded can be realized at a low cost.

2. Programming Method

Programming method using an N-type transistor is schematically illustrated in Fig. 1. Relatively large negative voltage ($V_{PGM}$) is applied to the gate with the S/D both set at 0 V. Because of the capacitive coupling between the gate and substrate, the potential in the surface of the substrate (called “channel region” hereafter) is negatively modulated. Consequently, reverse bias is effectively applied to PN junctions between the S/D and the channel region. At the same time the large band-bending in the gate-S/D overlap regions is caused by the high electric field between the gate and the S/D. When $V_{PGM}$ is sufficiently large, the potential differences between the S/D and the channel region exceed the breakdown voltage in PN junctions, and/or the band-to-band tunneling current is substantially enhanced because of the large band-bending aforementioned. Under those conditions, the PN junctions are successfully broken locally around the surface of the substrate, that is, the transistor is programmed to the on-state, in which the S/D are shorted.

3. Experiment and Analysis

The programming has been experimentally demonstrated. Fundamental experiments and analyses are performed using relatively large-EOT (equivalent oxide thickness) transistors (17 nm) with the gate length ($L_G$) of 1 μm. However, as discussed below, this method is also applicable to smaller-EOT and/or smaller-$L_G$ transistors in the same manner.

Figure 2 shows the change in the drain current ($I_D$) and the gate current ($I_G$) by applying $V_{PGM}$ to the gate. By applying $V_{PGM}$ of -28 V, irreversible on-state is obtained, in which the S/D are electrically shorted. On the other hand, there is no considerable change in $I_G$, that is, only local breakdown in PN junctions is successfully realized without deteriorating the gate dielectric. Figure 3 shows the drain-source current ($I_{DS}$) and the substrate-source current ($I_{SS}$) in the programmed switch. While ohmic conductivity is obtained in $I_{DS}$, $I_{SS}$ shows clear rectifying property. This means that the junction breakdown is not caused at the whole PN interfaces, but confined near the surface of the substrate.

The programming time ($T_{PGM}$) required for the formation of the conductive path depends on $V_{PGM}$ as shown in Fig. 4. Figure 4 shows the change in subthreshold swing (S.S.) when various $V_{PGM}$ is applied. The jump of S.S. means that the switch is successfully programmed. Even when the $V_{PGM}$ is applied to the gate, programming can be prevented by applying negative program-inhibit voltage ($V_{INH}$) to the S/D or staying them electrically floated as shown in Fig. 4.

Figure 5 shows an example of programming in a transistor array, in which $V_{INH}$ is applied to unselected cells.

In principle, $V_{PGM}$ and $T_{PGM}$ depend on EOT and impurity profiles around the S/D junctions. In contrast there is no dependence on $L_G$ as shown in Fig. 5. Figure 5(a) shows the change in S.S. in the smaller-$L_G$ transistor (150 nm) and Fig.
5(b) shows \( T_{\text{PGM}} \) when the conductive path is formed as a function of \( L_G \). Similar programming can be performed even in smaller-\( L_G \) transistors as well as in smaller-EOT devices. Figure 6 shows \( T_{\text{PGM}} \) dependences of \( I_D \) and \( I_G \) in a transistor with EOT of 6.4 nm. Reduction of \( T_{\text{PGM}} \) is attained due to small EOT, and \( V_{\text{PGM}} \) of -13 V is applied here.

For thorough understanding of the physical mechanisms, TEM (transmission electron microscope) images and elemental mapping profiles by EDX (energy-dispersive X-ray spectroscopy) are compared between the initial and programmed devices. Figures 7(a) to 7(c) are images of initial one, while Figs. 7(d) to 7(f) are those of programmed one. Although the transistor has Ni silicide electrodes on As-doped S/D, there is no considerable difference in As and Ni profiles between the initial and programmed devices. Furthermore, it is possible to apply this programming method to the devices not having Ni silicide electrodes as shown in Fig. 8. This means that the resistive change is not attributed to the particular elemental diffusion, but to local deterioration of Si crystallinity around the PN junctions.

4. Conclusion

Three-terminal one-time programmable switches using standard CMOS devices obtained by gate-controlled programming are demonstrated. The programmed switch has permanent conductive path between the S/D, which is created by the local breakdown in PN junctions. This method facilitates the design of peripheral circuits and does not require special manufacturing processes, which enables to realize the low-cost LSI with embedded one-time programmable switches.

References