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The Influence of Post-Etch InGaAs Fin Profile on Electrical Performance

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Abstract

The onset of the 22 nm node introduced 3-D Tri-Gate transistors into high-volume manufacturing for improved electrostatics. The next generations of Fin nMOSFETs are predicted to be InGaAs based. Due to the ternary nature of InGaAs, stoichiometric and structural modifications could affect the electronic properties of the etched Fin. In this work we have created InGaAs Fins down to 35 nm CD with atomic surface structure kept nearly identical to that of the bulk. Our experimental and simulation results show the impact of surface stoichiometry and Fin profile on electrical performance.

1. Introduction

With respect to the aspect ratio trapping technique [1-2], which deposits the III-V Fins from the bottom of the oxide trench, the dry etch process offers a top-down alternative. While the dry etch approach provides advantages such as process flexibility and simplicity, it may also introduce complications at the etched surface, including stoichiometric or structure modification and atomic intrusion. As a result, the electronic properties of InGaAs post etch could be modified. Mole fraction modification of In, for example, has been shown to vary the InGaAs charge neutrality level affecting device parameters such as the sub-threshold swing [3]. In this paper, defect-free III-V layers are used to study the impact of the etch parameters on the atomic composition as well as the electrical properties of the Fin sidewalls and the trench bottom.

2. Fabrication of the InGaAs Fin-MOSCAP

The fabrication starts with a 700 nm n-type $In_{0.53}G_{0.47}As$ layer lattice matched on (100) InP substrate (Fig. 1a). 50 nm of SiO_2 was used as etch HM (hardmask), shown in Fig. 1b. Fin patterns with different width and pitch were created using e-beam lithography. The HM and Fins were etched using the 2300® Kiyo C® Series conductor etch system (Lam Research). In Fig. 2, Fins with 49nm/97nm Fin width/height are shown with 87° angle and smooth sidewalls (X-SEM/TEM). The post-etch bottom surface shows slight roughness increase from 0.17 nm to 0.25 nm R_{RMS}. The samples received a surface treatment prior to the dielectric ALD (H_2O-based 4/4 nm Al_2O_3/HfO_2). 100 nm TiN was deposited as the gate electrode, formed by a lift-off process.

3. Physical analysis

The initial EELS (Electron Energy Loss Spectroscopy) results showed a redistribution of III-V surface composition on the Fin sidewall, which is significantly As rich with a thicker oxide layer. This is known to be responsible for surface Fermi-level pinning [4]. After optimizing the etch process the, EELS elemental maps in Fig. 3 reveal a balanced Fin sidewall surface stoichiometry, similar to that of the starting wafer surface with a thin oxide layer that is free of As. The bottom surface is In-rich, which facilitates a low bandgap compound formation, such as InAs and fuels In diffusion into the gate dielectric. The presence of In in ALD Al_2O_3 has been linked to oxide trapping in the InGaAs-Al_2O_3 MOS system [5].

4. Electrical analysis

CV characteristics: Fig. 4 shows the CV responses of the capacitors with an etched planar surface (4a) and an etched Fin structure (4b) using the optimized etch conditions. The former exhibits lower CV threshold voltage and stronger minority carrier response reflecting an In-rich surface, while the latter shows higher capacitance, steeper modulation and higher V_t indicating Fin sidewall contribution. Well-behaving response in the accumulation region indicates good electrical modulation. The CV 'shoulder' observed at 77K (Fig. 4c) could be the evidence of charge population in the higher-energy L-valley.

CV simulation: To further investigate this idea, we have developed a finite element code to solve the 2-D Schrödinger-Poisson equation self consistently. As shown in Fig. 5 the 2-D mesh is carefully tuned to cover the convexity of the Fin surface. Fig. 6 depicts the typical electron density at inversion regime. Due to high electric field at the top corner of the Fins, the carrier concentration peaks on the sidewall. On the contrary, the 2D potential profile at the bottom corner tends to expel carriers and the electron density is pinched off around those corners. As a result, instead of a uniform contribution from all the surfaces, the CV will be dominated by sidewall response. The simulation in Fig. 7 shows that the trench bottom contributes only about 15% of the capacitance. Fig. 8 details the movement of the chemical potential (Fermi-level) with respect to gate bias and energy above the conduction band minimum. The high electric field at the top corner of the Fins contributes to the occupation of the L valley subband and results in the CV shoulder characteristic.

5. Conclusion

InGaAs Fins with high aspect ratio were created with a sidewall surface structure nearly identical to that of the bulk. An In-rich trench bottom has been identified through physical and electrical analysis. The MOSCAP study shows well-behaving CV response and through simulation we find that the Fin sidewalls dominate the capacitance. Additionally, the observed CV shoulder response can be attributed to the population of the higher energy L valley

References

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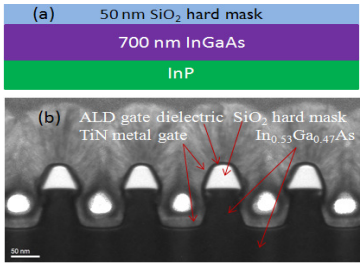

Fig.1 (a) Starting wafer: lattice matched n-type $In_{0.53}G_{0.47}As$ layer on InP with SiO2 hard mask; (b) TEM image of the final Fin MOSCAP structure completed with the ALD gate oxide and TiN metal top.

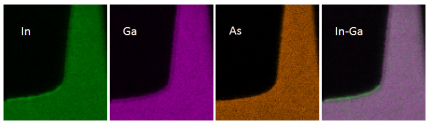

Fig.3 EELS elemental maps clearly show In-rich trench bottom, but balanced sidewall after Fin etch.

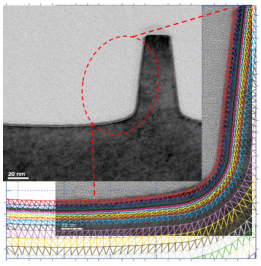

Fig.5 Meshing the actual Fin structure: The effective mass approx. with Dirichlet boundary condition is solved on Schrödinger solver domain (embedded in a larger Poisson solver domain), which extends up to 50 nm below the surface, where all the important wave functions will deminish

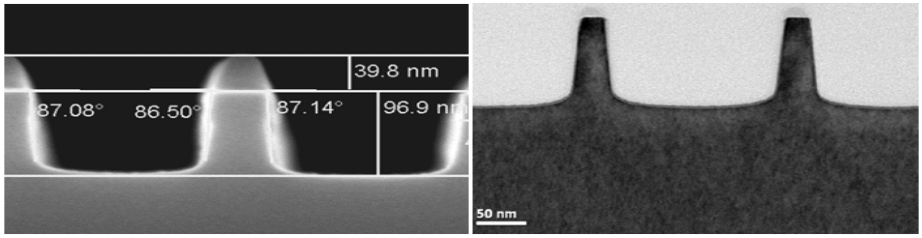

Fig.2 Cross-SEM and TEM micrographs of the etched fins. The cross-SEM picture shows the hard-mask and the etched Fin. The Fins are of 50 nm width and 97 nm height with 87 degree sidewall angle. The TEM (right) graph illustrates another Fin structure of 35 nm width and 100 nm height with smooth sidewalls.

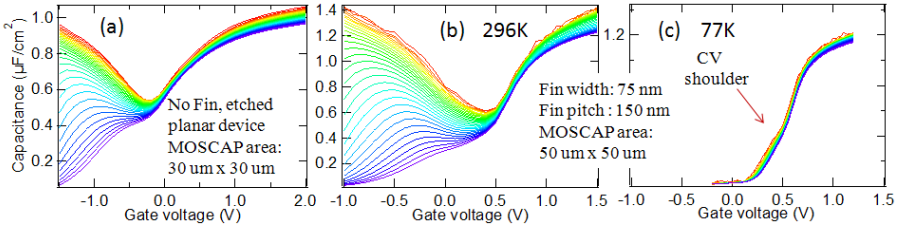

Fig.4 (a) CV traces of the etched (100 nm recess) planar MOSCAP. Lower threshold voltage and strong minority carrier response at negative bias reflect higher In content of the etched bottom surface. (b) Room temperature CV response of the Fin MOSCAP includes the contributions of the Fin sidewalls and the trench bottom. (c) Same device measured at 77K. Notice the CV shoulder at 0.5V gate bias. This shoulder is likely due to the population of the L valley, which has a higher energy level and heavier effective mass.

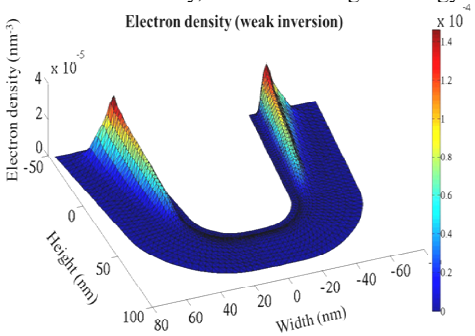

Fig.6 The Fin sidewalls and top corners dominate in inversion charge density due to high electric fields while the bottom trench and corners remain depleted due to convexity. The structure has a 150 nm pitch and 75 nm Fin width with gate electrode and dielectric on the Fin sidewalls and the trench bottom surface.

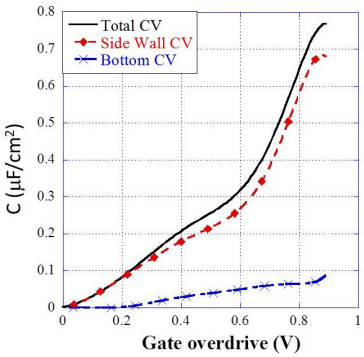

Fig.7 The simulated contribution of different surfaces. Notice the CV shoulder at 0.6V due to the occupation of the first subband of L valley.

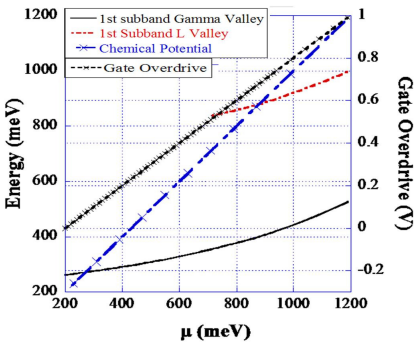

Fig.8 The energy of first subband from Γ and L valley for different bias. The increas of the gate overdrive pushes the chemical potential (μ) deeper into the conduction band. For a 800 meV offset between μ and the minimum of the Γ valley, the first subband of L valley starts to be occupied. This translates into a 0.6V gate overdrive and results in a steep shoulder in CV around the same bias point.