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Bulk FinFET Fin Height Control using Gas Cluster Ion Beam (GCIB) – Location Specific Processing (LSP)

Min-Soo Kim[1], Romain Ritzenthaler[1], Jean-Luc Everaert[1], Luis Fernandez[2], Katia Devriendt[1], Jae Woo Lee[1], Augusto Redolfi[1], Sofie Mertens[1], Ed Burke[2], Naoto Horiguchi[1], and Aaron Thean[1]

[1] imec, Kapeldreef 75, 3001 Leuven, Belgium, min-soo.kim@imec.be
[2] Tokyo Electron, Kapeldreef 75, 3001 Leuven, Belgium.

Abstract

We report a Gas Cluster Ion Beam (GCIB)-Location Specific Processing (LSP) in order to reduce fin height variability in a gate-first bulk finFET integration flow. A statistical analysis of inline and electrical parameters is conducted to access the impact of GCIB-LSP. It is found that at wafer level the variability is significantly improved by the GCIB-LSP.

1. Introduction

In recent years, FinFETs fabricated on bulk wafers ("Bulk FinFETs", bFF) emerged as a pragmatic solution to provide pace for further downscaling (22/14 nm node) [1]. When V_{DD} scales below 1.0 V, device variability has become a major concern for CMOS technology. We reported device impact of fin height (finH) variation [2,3] could be responsible up to 15% of drive current (I_D) within wafer (WiW). Therefore, finding a technique to reduce its variation is a prime interest for bFF technology. In this report, GCIB-LSP is employed to improve nitride (SiN) and field oxide (F_{ox}) films layer thickness uniformity to realize a reduction of the finH variation. LSP was performed using the TEL Epion nFusion GCIB system installed in the imec 300mm cleanroom. Variability is assessed using inline metrology, and correlated to electrical measurements.

2. Device Fabrication

The details of fin formation and overall integration flow for bFF devices are illustrated in Fig. 1a and 1b, respectively. Possible sources of variability of this report are illustrated in Fig. 1c. As depicted in Fig. 1d, SiN hard-mask (HM) thickness post shallow trench isolation (STI) chemical mechanical polishing (CMP) is an onset of subsequent finH variation. Therefore, GCIB-LSP right after the CMP to achieve more uniform SiN thickness would result in a reduction of the finH variation. Fig. 2 illustrates a typical edge-thin SiN HM profile right after STI CMP, and a *flattened* SiN thickness by GCIB-LSP. It not only changed profile of nitride films at the edge (radius > 120mm), but also improved 3σ of SiN films thickness from 1.5 to 0.6 nm, excluding the edge from a full wafer mapping. The 1st F_{OX} recess target was adapted to cope with different incoming SiN thickness. After the fin formation, a typical gate-first (GF) high-κ/metal gate (HK/MG) CMOS integration process follows. In order to conclude about a change of electrical performance correlated to the inline improvement of finH using the GCIB-LSP, the convoluted effects of fin length, fin width, gate length, gate dielectric thickness t_{inv} and mobility μ_e have to be assessed. Among those, inline critical dimension (CD) data of finW, and gate length (L_G) of our nominal 5-fin device for the samples with and without GCIB-SLP are analyzed as shown in Fig. 3. Their values are statistically identical for the regions covered by the measurement. Considering all the wafers has seen the same junction implants and gate stacks, we're certain the device variations from this report is mostly from finH.

3. Electrical Characterization and Discussion

Metrology is critical in bFF baselines, since most of electrical Figures Of Merits (FOMs) have to be normalized by the fin dimensions. The gate leakage J_G at V_{TH}+0.6V is a function of fin dimensions and gate dielectric thickness t_{inv}. On a long and narrow devices, similar *non-normalized* I_G (Fig. 4; unit:A) obtained for all wafers indicates that the gate dielectric thickness is not changed applying GCIB-LSP. Knowing that, we can now investigate if this finH is translated into a better variability in I_D performance. First, we considered a long channel (negligible external resistance effect) in the linear regime (no velocity saturation) and extracted the *normalized* $I_{D,lin}$ at V_G+1V multiplied by t_{inv} across the wafer (to account for the t_{inv} variations on wafer edge) as one of the FOMs as shown in eq. (1):

$$I_{D,lin} \times t_{inv} @V_{TH,lin} + 1.0V \qquad (1)$$

Using the lognormal cumulative plot of this FOM (Fig. 5, L_G=1µm, finW=30nm), it clearly appears that the variability is significantly improved on GCIB-LSP samples (it is noteworthy that the repeatability wafer to wafer is excellent of the 4 processed GCIB-LSP samples). Similar measurements carried out on short channels in the saturation regime (Fig. 6, L_G=40nm, V_{DS}=1V) lead to similar conclusions. It demonstrates that the variability improvement obtained with the GCIB-LSP technique is not impeded by Short Channel/Saturation Effects, and can be beneficial in the real device operation conditions.

However, it is also very clear considering Figs. 5 and 6 that the I_D is reduced on GCIB-LSP samples. The reason could be a drop of the μ_e during the GCIB-LSP, possibly due to an implant-like damage component. Since GCIB-LSP was applied on top of SiN HM after the STI CMP, a μ_e degradation should primarily affect the top channel. This is checked by plotting $I_{D,lin}$ on long and wide device (finW=1µm) as shown in Fig. 7, where no degradation (median values exhibit 6% difference) is observed for GCIB-LSP samples. GCIB-LSP is therefore not degrading μ_e. This conclusion is further supported by the low frequency noise (LFN) measurements (Fig. 8). Traps in HK/SiO_2/Si layers might be introduced during GCIB-LSP and remain even after the gate oxide formation which is normally followed by a sacrificial oxidation. Normalized noise spectrum (S_{ID}/I_D^2) (at f=1Hz, averaged on 3 dies) is following the $(g_m/I_D)^2$ trend and shows that the major noise mechanism is based on carrier number fluctuations, allowing the trap density (N_t) extraction [5]. The N_t is extremely similar with and without GCIB-LSP, both for narrow and wide devices (Fig. 8). Benchmarking the extracted trap density with various HK/MG integration options, it is clear that GCIB-LSP sample are well on trend with previously reported data. Having discarded a μ_e degradation using the GCIB-LSP, the most likely source for the I_D degradation is actually the metrology itself, with a small discrepancy between measured inline and real data yielding improper normalization. It could be induced by modification of F_{OX} surface during the GCIB-LSP, which in turn would lower the oxide etch rate during the F_{OX} recess step.

4. Conclusions

It is shown that the fin height variation at wafer level can be greatly reduced using the GCIB-LSP. This finH variability improvement is translated into a better variability of I_D, including in the real operation conditions. Through a detailed analysis of device parameters (V_{TH}, I_D, t_{inv}, μ_e, N_t), it is shown that GCIB-LSP is an electrically benign technique to reduce WiW finH variation; the great potential of this technique will contribute to further scaling of advanced bFF technologies, where the variability is a serious challenge to be tackled.

Acknowledgements

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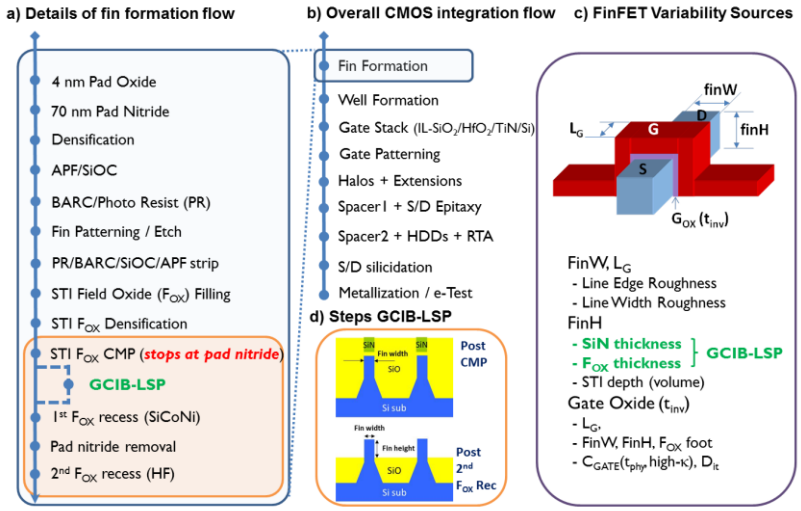

Fig. 1 Process flow of bulk finFET device fabrication (a, b); sources of inline process variation (c); and process step where GCIB was applied to reduce finH variation (d).

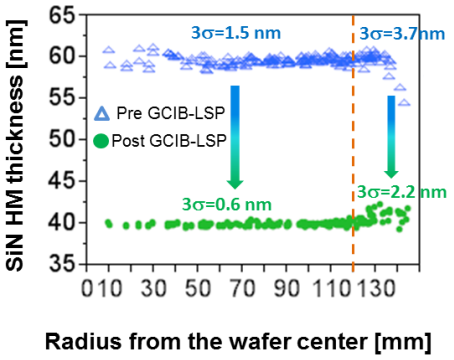

Fig. 2 Nitride thickness profile measured before (=right after the STI CMP, open symbols) and after (closed symbols) the GCIB-LSP, showing typical edge-thin nitride profile before the GCIB-LSP and *flattened* nitride thickness profile after the GCIB-LSP. 3σ values from two regions (edge: radius > 120mm; inner: radius <= 120mm) separated by dotted lines clearly shows GCIB-LSP not only improved location specific thickness variations, but also improved global thickness variations.

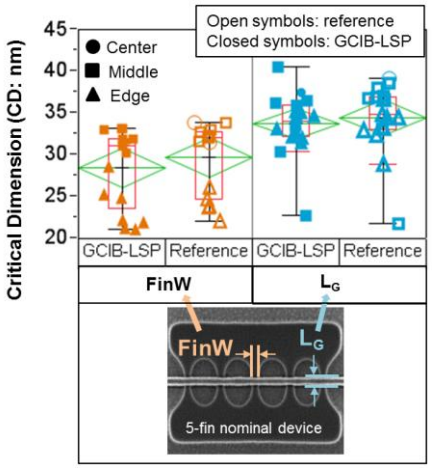

Fig.3 Inline CD data of finW and gate length (L_G).

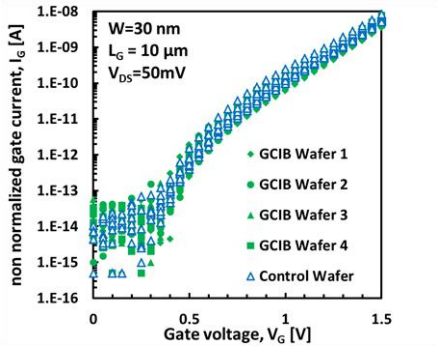

Fig. 4 Gate current I_G vs. gate voltage V_G for bFF with (closed symbols) and without (open symbols) GCIB-LSP correction. FinW=30nm, L_G = 10 µm.

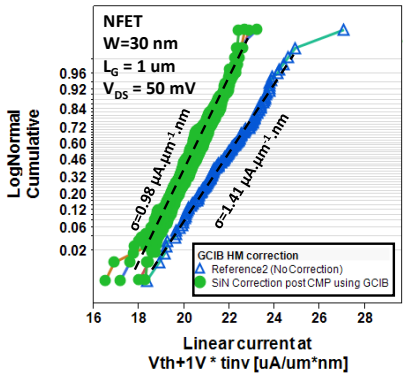

Fig.5 Linear drive current*t_{inv} at offset V_{TH} with (closed symbols) and without (open symbols) GCIB-LSP correction. FinW=30nm, L_G = 1 µm.

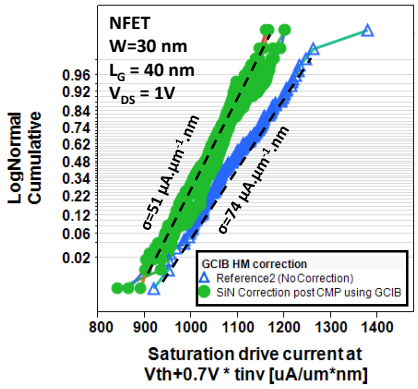

Fig.6: Saturation drive current*t_{inv} at offset V_{TH} with (closed symbols) and without (open symbols) GCIB-LSP correction *on short channel transistors*. FinW=30nm, L_G = 40 nm, V_{DS}=1V.

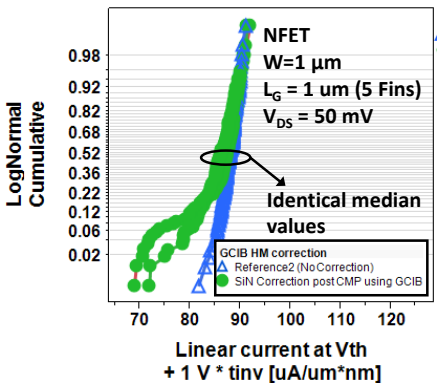

Fig. 7: Linear drive current*t_{inv} at offset V_{TH} with (closed symbols) and without (open symbols) GCIB-LSP correction. finW=1µm, L_G = 1 µm.

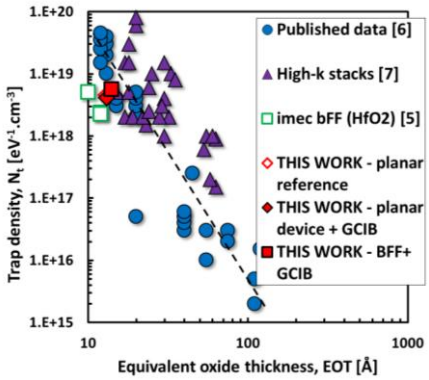

Fig. 8: Trap density extracted from Low Frequency Noise spectral density vs. EOT.