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New Observations on the Corner Effect and STI-Induced Effect in Trigate CMOS Devices

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Abstract- This paper reports the impact of the corner effect and STI-induced effect on the reliability of 28nm bulk trigate devices. It was found that corner effect in nMOS trigate devices is an important factor, which results in an obvious degradation in the middle of the channel after the hot carrier (HC) stress. The induced degradation is strongly related to the geometry of trigate devices. And, it was found that as the fin size continuously shrinks, the corner effect is enhanced and should be treated carefully. Moreover, it was also found that the narrower STI enhances NBTI-induced degradation in pMOS devices, and the taller the fin height is, the worse the NBTI-induced degradation becomes. Finally, a guideline has been proposed to alleviate the corner effect in enhancing the reliability of trigate devices. These results provide valuable information for reliable design of future generation trigate devices.

1. Introduction

As devices are scaled down, the bulk trigate CMOS devices have been employed as the mainstream beyond 22nm node [1]. Although the performance and variability of bulk trigate devices have been studied extensively [2-4], the reports on the reliability of this kind of devices are quite limited [5]. The previous study revealed that the corner in the fin structure of the trigate devices degrades the performance of devices [5]. But the mechanisms of such effect are still unclear. In this work, we are interested in understanding how the corner is involved in the degradation of reliability for trigate devices after hot carrier stress for nMOS devices and how the surface-roughness of fins impact on the NBTI degradation for pMOS devices. Based on our recently developed technique, random trap profiling [6], the trap density along the channel direction can be evaluated, which allows us to further understand the trap generation after the stresses. Then, the correlation between the corner/STI effects and the stress will be elaborated.

2. Device Preparation

Poly-Si gate bulk trigate devices, with SiON insulator, were fabricated. The schematic cross section diagram of trigate CMOS device is shown in Fig.1. The width of trigate device is 45nm and the mask channel length is 36nm; the effective channel length is 24nm. To exclude the parasitic effects, single-fin devices have been used as the test samples.

3. Results and Discussion

A. Methodology of Random Trap Profiling Technique (RTP)

To find the positions of oxide traps in the channel, the distributions of random trap densities in the channel can be characterized by the random trap profiling technique (**RTP**) []. The main idea of RTP is described below. If the discrete trap is treated as a delta function located in the channel, only those discrete traps at the channel barrier peak affect the carrier transport and fluctuates the V_{th}.(Fig.2) By increasing the source-to-drain voltage, V_{sd}, the channel barrier peak will be moved from the middle of the channel to the region near the drain side(Fig.3), from which we can calculate the trap density as a function of the channel position from the measured V_{th}.

B. Corner Effect Induced Degradation in nMOSFETs

To understand the corner effect enhanced degradation, Fig. 4 shows the trap density along the channel direction under HC stresses with different vertical electric fields but the same horizontal field. The trap peaks near the drain grow as the vertical field rises due to the stronger electric field near the drain. Fig. 5 shows the trap density after HC stress with different horizontal fields but the same vertical field. The trap in the middle of the channel increases since the field is more concentrated around the corner of the fin. From the results of Figs. 4&5, the corner effect is strongly dependent on the horizontal field, which exhibits different trap distributions for planar devices (only the peaks near the drain) and trigate devices (also the damage in the channel middle), as in Fig. 6. More importantly, the corner effect enhances the degradation caused by the HC stress, Fig. 7 and Table 1.

To alleviate the corner effect, the geometry of fin structure has been examined. First, different fin heights of devices were prepared (Fig. 8) and it was found that the shorter the height is, the higher the magnitude of trap density near the channel becomes, which is because there is a stronger field in the shorter Fin, and the field is more dense around the corner with respect to the taller Fin, (Fig. 9). As a result, the small fin gives rise to serious degradation caused by the corner effect in trigate nMOS devices. In short, to reduce the corner effect, it is suggested to increase the source/drain resistance (R_{sd}), Fig.10. Since the magnitude of the electric field in the channel will be reduced by the exterior S/D resistance on the fin, it was found that the trap density after HC stress for high R_{sd} gives a lower degradation than that for lower R_{sd}. (Fig.11)

C. STI Induced NBTI Stress Effect in pMOSFETs

In our specific structure with an STI to define the fin, what is interested to us is the geometry and structure of fins? Fig. 12 shows the different space-lengths between two fins, which are insulated by STI. It was found that the narrower the space is, the more degradation the devices after NBTI stress becomes. The reasons may be attributed to the corner between STI and the fin.(Fig.13) The narrower the STI is, the stronger the filed intensity around the corner between STI and channel becomes. Since a narrower STI will induce a sharp corner between STI and the fin, which then generate a higher electric field around the corner and finally worsens the surface-roughness of the fin. In order to understand the issue, Fig. 14(a) shows the results of different fin-heights but the same space between fin and fin of devices suffered from NBTI stress. It was found that the taller the fin-height is, the more degradation can be observed, which could be explained by the surface roughness caused by the field intensity around the STI corner, and taller fin maintains more strength of field for the STI corner, compared to the shorter fin. If the amount of interface traps of devices after NBTI stress is plotted against the fin heights, The amount of interface traps contributed by the fin-width only can be obtained, Fig. 14(b). The result shows that the amount of traps coming from the fin width is minor with respect to that from the fin height.

In summary, the corner and STI induced reliability related to the fin geometry in trigate devices has been analyzed. It was found that the corner effect is strongly dependent on the transverse field, and also will be enhanced in a small fin structure. Finally, we have successfully proposed a structure of higher R_{sd} fin to alleviate the corner effect. On the observation of NBTI in pMOSFETs, it was also found that a narrower STI may degrade the NBTI reliability due to the stress effect around the corner between the STI and the channel. All these results will be valuable to understand the physical insights and to design more reliable trigate devices.

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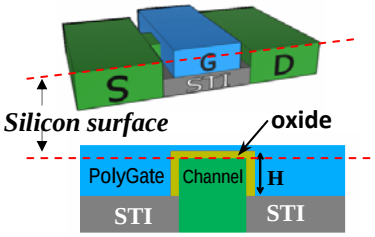


Fig. 1 (*top*) The 3D structure of bulk trigate devices with poly/SION gate ; (*bottom*) the cross-sectional view of bulk trigate devices with fin height H.

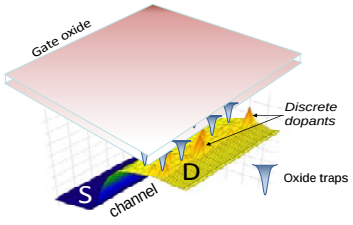


Fig. 2 For fresh devices, the discrete dopants in the channel cause the variation of the threshold voltage. For stressed devices, the interface-trap induced trap barriers will also give rise to the threshold voltage variation.

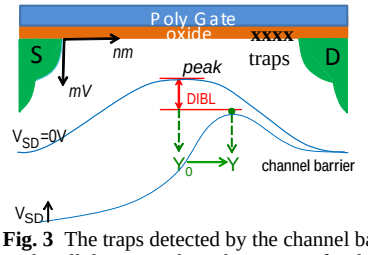


Fig. 3 The traps detected by the channel barrier peak will dominate the Vth variation for the device after the stress. By varying the Vsd, the barrier peak will be shifted toward the drain such that the trap density can be profiled along the channel.

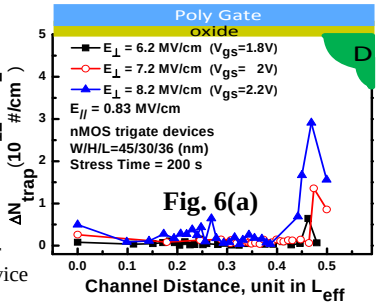
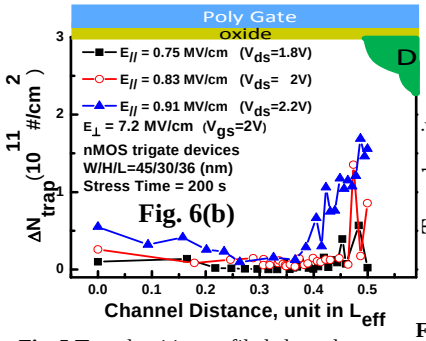


Fig. 4 Trap densities along the transverse direction of channel after different vertical electric fields but constant transverse field. Note that the stronger the vertical field is, the higher the peak near drain side becomes.



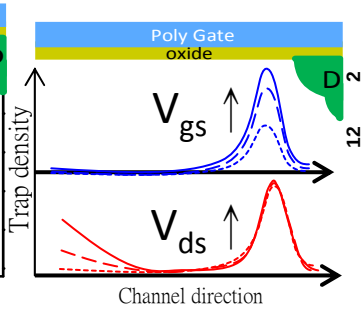


Fig. 6 The trap distributions after different HC stress schemes. For increase of Vgs, the peak near drain side grows. For increase of Vds, the region near channel middle grows.

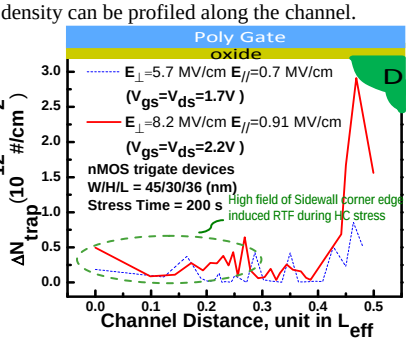


Fig. 7 The trap densities along the channel direction after strong or week HC stress. It was found that the peaks are not only near the drain edge but also in the channel region after HC stress, and the stronger the HC stress is, the higher they becomes.

The average trap density@ Stress Time = 200 s	Average increased trap density (cm^{-2})		
	Channel middle	Drain Edge	Channel middle / Drain Edge(%)
E = 5.7 MV/cm (V_{GS}=V_{DS}=1.7V)	1.62×10^{11}	3.53×10^{11}	46%
E = 8.2 MV/cm (V_{GS}=V_{DS}=2.2V)	3.13×10^{11}	1.05×10^{11}	30%

Table 2 The comparison of the generated trap densities for trigate devices after HC in different stress condition, showing that corner effect was more important as stress field decreases.

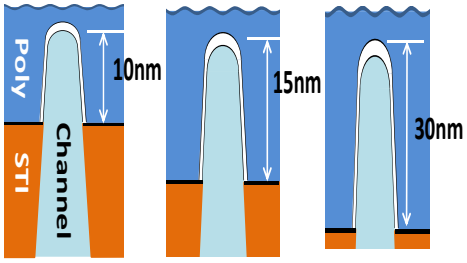
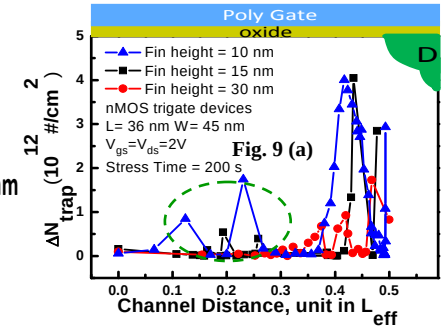


Fig. 8 To study the impacts of the sidewall on the degradation of stressed trigate devices, three different sidewall devices were prepared.



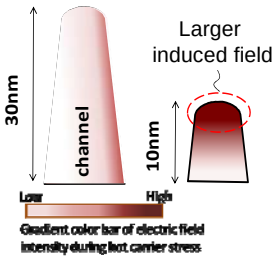


Fig. 9 (b)

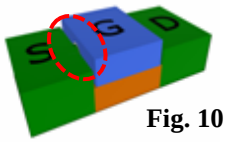


Fig. 10 (a)

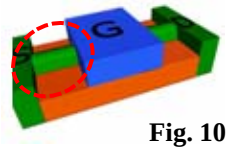


Fig. 10 (b)

Fig. 9 (a) ΔN_{trap} profiling for different Fin-height trigate devices after HC stress. More traps are observed for lower Fin-height device as a result of larger electric field. (b) The illustration of the high electric field at the low fin height device which will induce larger electric field in devices under HC stress.

Fig. 10 The illustration of two different bulk trigate devices with (a) low R_{sd} (the covered Fin), (b) high R_{sd} (the uncovered Fin).

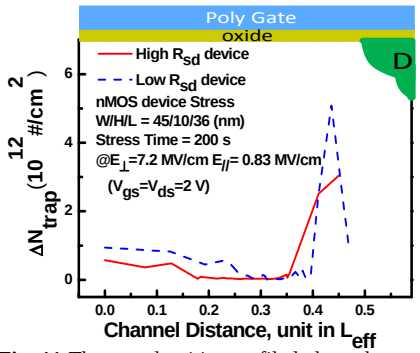
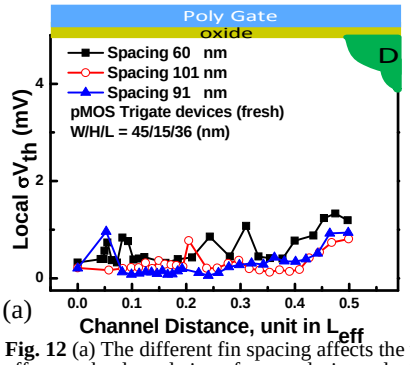


Fig. 11 The trap densities profiled along the transverse direction of channel. Since the electric field in the channel can be reduced by the exterior S/D resistance on the fin, it was found that the trap density after HC stress for high Rsd shows a low degradation than that for lower Rsd..



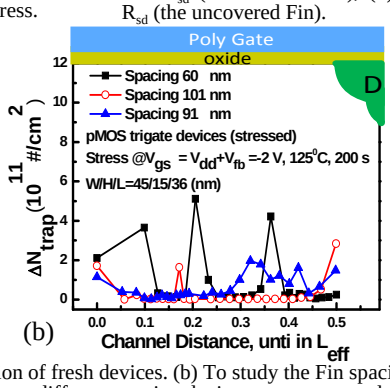


Fig. 12 (a) The different fin spacing affects the variation of fresh devices. (b) To study the Fin spacing effect on the degradation of stressed trigate devices, three different spacing devices were measured.

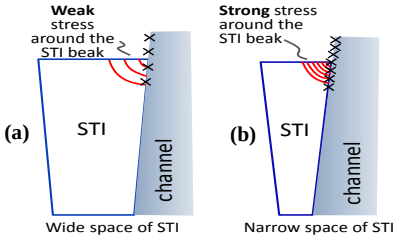
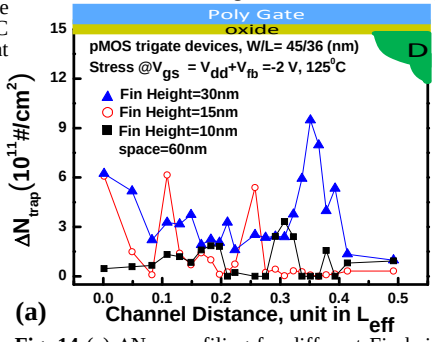


Fig. 13 (a) The illustration of a wide STI; (b) the illustration of a narrow STI. The narrower the STI is, the stronger the filed is around the corner between STI and channel.



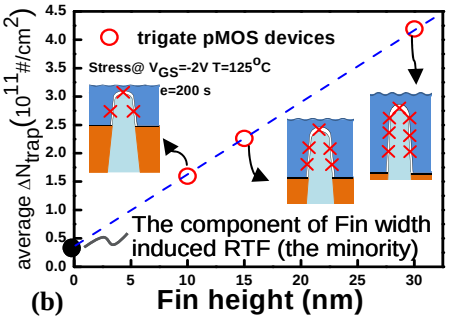


Fig. 14 (a) ΔN_{trap} profiling for different Fin-height trigate devices after NBTI stress. More traps are observed for larger Fin-height device as a result of sidewall roughness effect. (b) Interface trap density of Fin structure was measured by different fin-heights devices. The amount of interface traps contributed by the fin-width only can be obtained from the plot by extrapolating the measured data to zero fin-height.