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Leakage-Delay Analysis of $In_xGa_{1-x}As$-OI FinFETs for Logic Applications

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Abstract

This paper analyzes the impacts of different high threshold voltage techniques on the leakage-delay of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs compared with the SOI counterparts. The Band-To-Band Tunneling (BTBT) leakage triggered bipolar effect needs to be taken into account for the $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs. Due to its smaller band-gap and effective mass, the BTBT induced bipolar current is larger in the $In_{0.7}Ga_{0.3}As$-OI FinFET than in the $In_{0.53}Ga_{0.47}As$-OI FinFET. The Ioff of $In_xGa_{1-x}As$-OI FinFETs can be reduced by drain-side underlap while the source-side underlap is less effective. $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs with drain-side underlap exhibit better leakage-delay performance compared with source-side underlap and increasing gate length.

Introduction

FinFET has emerged as the prime candidate for extremely scaled MOSFETs due to its superior control of Short-Channel Effects (SCE) [1, 2]. $In_xGa_{1-x}As$ MOSFETs with high mobility are attractive candidates for replacing strained Si channels. However, due to its high permittivity and low band-gap, $In_xGa_{1-x}As$ MOSFET suffers from SCE and Band-To-Band Tunneling (BTBT) leakage. Combining the advantages of the FinFET structure and the high mobility of $In_xGa_{1-x}As$ becomes a promising approach for future high-performance MOSFETs [3, 4].

The In-rich $In_{0.7}Ga_{0.3}As$ channel offers higher mobility and on-current than $In_{0.53}Ga_{0.47}As$ MOSFET [4-6]. In this work, the leakage-delay characteristics of $In_{0.53}Ga_{0.47}As$-OI and $In_{0.7}Ga_{0.3}As$-OI FinFETs are examined and compared with the SOI counterparts. Three high threshold voltage (Vt) techniques including increasing gate length (Lg), drain-side underlap (Lund), and source-side underlap (Luns) are compared.

Device Design and Simulation Methodology

Fig. 1 shows the schematic of $In_xGa_{1-x}As$-OI FinFET and the device parameters used in this work. The material parameters for $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As$ are listed below: band-gap (Eg) = 0.74eV/0.58eV [7, 8], effective mass (m*) = $0.041m_0/0.034m_0$ [7, 9], permittivity (ε) = 13.9/14.3 [7], affinity (χ) = 4.05V/4.65V [7]. The reduced effective mass [10] for Band-To-Band Tunneling (BTBT) is calibrated for $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$, respectively. The band-gap widening due to quantum confinement is considered for the 7nm fin width $In_xGa_{1-x}As$-OI FinFETs.

Fig. 2 shows the Ids-Vgs characteristics for $In_{0.53}Ga_{0.47}As$-OI, $In_{0.7}Ga_{0.3}As$-OI and SOI FinFETs at Vds = 1V and 0.05V. $In_{0.53}Ga_{0.47}As$-OI, $In_{0.7}Ga_{0.3}As$-OI and SOI FinFETs are designed with same threshold voltage (Vt) at Vds = 1V. $In_{0.7}Ga_{0.3}As$-OI FinFETs with smaller band-gap and effective mass exhibit larger on-current and leakage current at Vds = 1V compared with the $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs.

BTBT induced Bipolar Effect in $In_xGa_{1-x}As$-OI FinFETs

Fig. 3 shows the lateral band diagrams of the $In_{0.7}Ga_{0.3}As$-OI FinFET at Vgs = 0V and Vds = 1V. A significant band overlap between the channel and drain regions for $In_{0.7}Ga_{0.3}As$-OI FinFET results in band-to-band tunneling across the drain-channel junction. The electrons tunnel from the valence band of the channel to the conduction band of the drain, leaving behind holes in the channel region (Ib,hole). For $In_xGa_{1-x}As$-OI FinFET, the generated holes accumulate in the channel, causing forward bias of the source-channel junction and eventually turning on the bipolar effect [11] to induced an amplified BTBT current (β xIb,hole). Fig. 4 shows that the total Ioff for $In_xGa_{1-x}As$-OI FinFET equals the sum of [(β +1) x Ib,hole] and the subthreshold leakage (Isub-vt).

Fig. 5 shows the leakage components of the $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs at various Vds. For $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs, the total leakage Ioff is dominated by the amplified BTBT current (β xIb,hole) at Vds > 0.6V, and dominated by the Isub-vt at Vds < 0.6V.

Leakage-Delay Analysis

Power-performance optimization requires devices with multiple Vt [12]. Several device designs can be used to achieve high-Vt. Asymmetric gate-to-source/drain underlap devices have been used in SRAM cell to improve the cell leakage and stability [13]. Increasing gate length was commonly used in microprocessor design [14]. Fig. 6 shows the schematics of low-Vt (LVT) and high-Vt (HVT) FinFET including increasing gate length (Lg), drain-side underlap (Lund) and source-side underlap (Luns). The effective drive current (Ieff), which more accurately predicts digital circuit performance [15], is used to assess the device performance. Intrinsic delay, (CggxVdd/Ieff), is used to assess the circuit performance, where Cgg is the total gate capacitance. Fig. 7 shows the Cgg vs. Vgs characteristics for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs using Poisson-Schrödinger simulations. As can be seen, $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs show much smaller quantum capacitance [16] due to their smaller effective mass and low density of states.

Fig. 8 shows the impact of varying Lg on the leakage, Ieff and delay for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs at Vdd = 1V. For $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs, the BTBT currents (Ib,hole) are not sensitive to Lg. The BTBT induced bipolar currents (β xIb,hole) dominate the Ioff of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs, and bipolar gain β becomes larger as the channel length decreases. The Ioff of SOI FinFETs dominated by the subthreshold leakage shows much larger Lg dependence compared with the $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs. Fig. 8(b) shows the intrinsic delay (CggxVgg/Ieff) decreases as Lg increases (ΔLg > 0) due to the reduced Ieff and increased gate capacitance. Fig. 9 shows that the Ioff of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs exhibit larger dependence on the drain-side underlap length compared with the SOI FinFET. As ΔLund increases, the Ieff decreases and the gate-sidewall capacitance decreases. Therefore, the delay performance of $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with ΔLund = 6nm (Fig. 9(b)) are better than that with ΔLg = 6nm (Fig. 8(b)).

Fig. 10 shows that for $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs, increasing source-side udnerlap only shows slight decrease in Ioff. Fig. 10(b) shows that $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with Luns show smaller Ieff and larger delay than that with Lund. Due to more drain field coupling into the channel region, increasing Lund results in lower Vt, larger Ieff and therefore smaller delay compared with increasing Luns. Fig. 11 compares the leakage-delay for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs at Vdd = 1V and 0.8V. As Vdd decreases from 1V to 0.8V, the Ioff reduction of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs is larger than that of SOI FinFET. Fig. 12 shows that for $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs, increasing ΔLund shows larger Ioff reduction compared with increasing ΔLg and ΔLuns, while for SOI FinFET, increasing ΔLg shows larger Ioff reduction. Fig. 13 compares the leakage-delay of $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with different HVT techniques. $In_{0.7}Ga_{0.3}As$-OI FinFET with ΔLund = 4nm shows comparable leakage and smaller delay compared with the $In_{0.53}Ga_{0.47}As$-OI with ΔL = 0. SOI FinFETs with ΔLg = 4nm shows comparable delay and smaller Ioff compared with the SOI FinFETs with ΔLund = 6nm.

In summary, due to its smaller band-gap and effective mass, the BTBT induced bipolar leakage current is larger in $In_{0.7}Ga_{0.3}As$-OI FinFET than in $In_{0.53}Ga_{0.47}As$-OI FinFET. $In_{0.7}Ga_{0.3}As$-OI FinFET with Lund exhibit comparable Ioff and smaller delay than $In_{0.53}Ga_{0.47}As$-OI FinFET.

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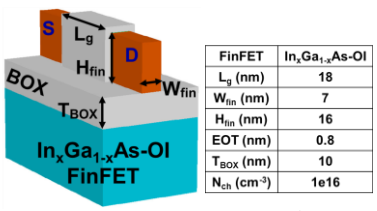


FinFET	$In_xGa_{1-x}As$-OI
L_g (nm)	18
W_{fin} (nm)	7
H_{fin} (nm)	16
EOT (nm)	0.8
T_{BOX} (nm)	10
N_{ch} (cm^{-3})	1e16

Fig. 1. Schematic of $In_xGa_{1-x}As$-OI FinFET, and the device parameters used in this work. ($In_xGa_{1-x}As$-OI: x=0.53 and 0.7)

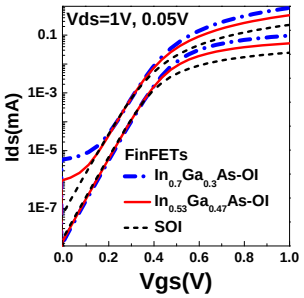


Fig. 2. Ids-Vgs characteristics of $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI, and SOI FinFETs at Vds=1V and 0.05V.

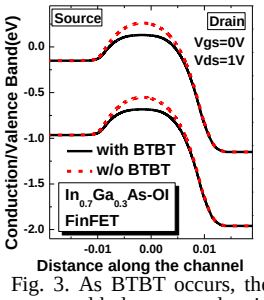


Fig. 3. As BTBT occurs, the generated holes accumulate in the channel resulting in a forward bias across the source-channel junction.

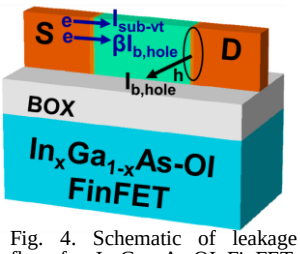


Fig. 4. Schematic of leakage flow for $In_xGa_{1-x}As$-OI FinFET. As BTBT occurs, a hole flux (Ib,hole) flows into the channel region which triggers the bipolar effect and induced an amplified BTBT current (β xIb,hole).

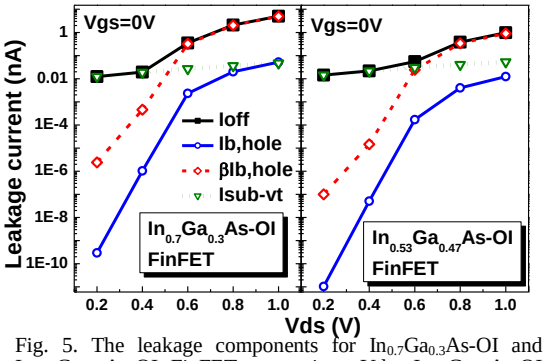


Fig. 5. The leakage components for $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs at various Vds. $In_{0.7}Ga_{0.3}As$-OI FinFET shows larger Ioff than $In_{0.53}Ga_{0.47}As$-OI FinFET at Vds=1V.

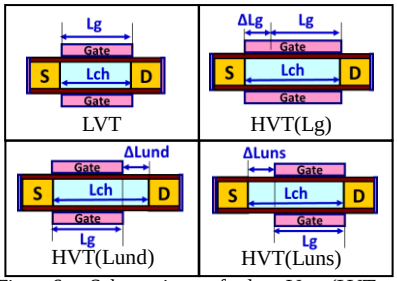


Fig. 6. Schematics of low-Vt (LVT, Lg=18nm) and high-Vt (HVT) FinFETs options using drain-/source-side underlap (Lund/Luns), and increasing gate length (Lg).

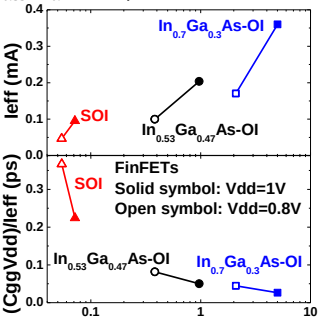
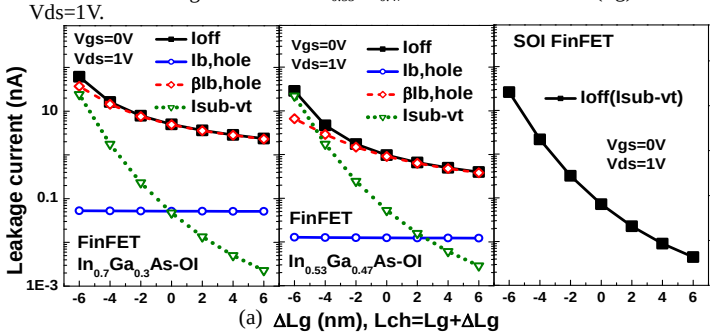


Fig. 7. Cgg vs. Vgs characteristics of LVT (Lg=18nm) $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI, and SOI FinFETs.



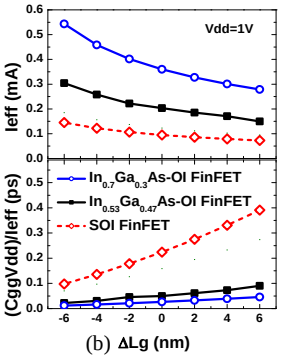
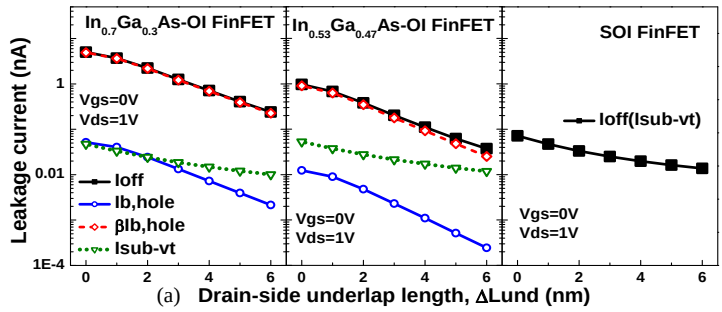


Fig. 8. (a) The leakage components and (b) Ieff/delay for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with various ΔLg at Vds=1V. Channel length Lch=Lg(18nm)+ΔLg. The definition of Ieff is $(I_{high}+I_{low})/2$, where I_{high} equals the on-current at Vgs=Vdd and Vds=Vdd/2, and I_{low} equals the on-current at Vgs=Vdd/2 and Vds = Vdd.



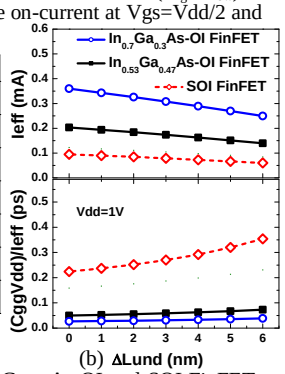
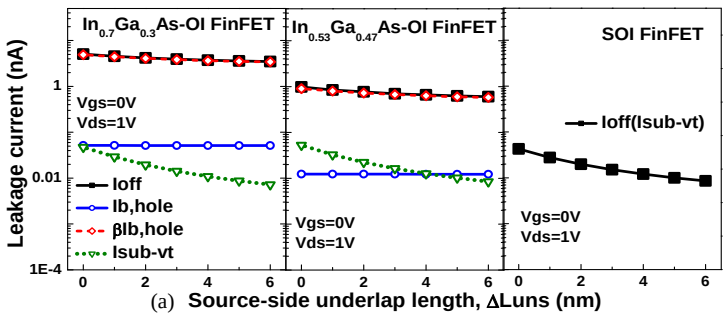


Fig. 9. (a) The leakage components and (b) Ieff/delay for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with various ΔLund at Vds=1V. Channel length Lch=Lg(18nm)+ΔLund. The leakage currents of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs show larger Lund dependence compared with the SOI FinFET.



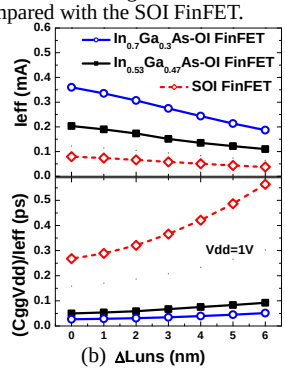


Fig. 10. (a) The leakage components and (b) Ieff/delay for $In_{0.7}Ga_{0.3}As$-OI, $In_{0.53}Ga_{0.47}As$-OI and SOI FinFETs with various ΔLuns at Vds=1V. Channel length Lch=Lg(18nm)+ΔLuns. The leakage currents of $In_{0.7}Ga_{0.3}As$-OI and $In_{0.53}Ga_{0.47}As$-OI FinFETs cannot be reduced effectively by increasing ΔLuns.

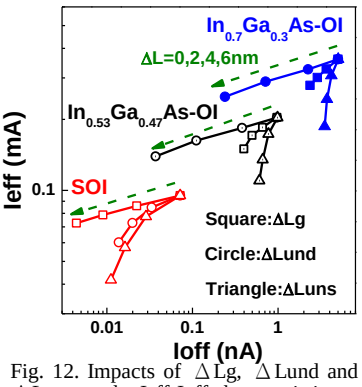


Fig. 12. Impacts of ΔLg, ΔLund and ΔLuns on the Ieff-Ioff characteristics at Vdd=1V.

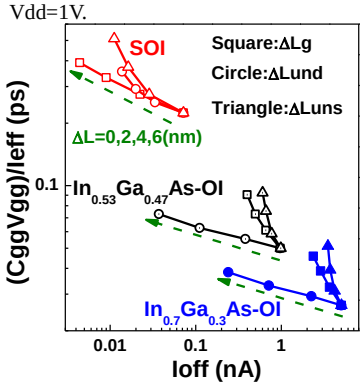


Fig. 13. Impacts of ΔLg, ΔLund and ΔLuns on the leakage-delay characteristics at Vdd=1V.