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Comparison of Analog FOM for TFET and FinFET Considering Work Function Variation

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Abstract

This work investigates and compares the impacts of metal-gate work function variation (WFV) on the analog FOMs (figure of merits) for TFET and FinFET devices using 3-D atomistic TCAD simulations. Our results indicate that at V_D = 0.6 V, TFET can provide a significantly larger output resistance (R_{out}) and thus a better intrinsic gain than FinFET. In addition, TFET exhibits better immunity to WFV in terms of g_m/I_D, R_{out} and intrinsic gain (g_mR_{out}) than the FinFET counterparts. Our study may provide insights for low-voltage analog design using TFET technologies.

I. Introduction

Tunnel FET (TFET) is regarded as one of the most promising device candidates for future ultra-low power applications [1]. Using band-to-band tunneling as the major conduction mechanism, TFET enables steeper subthreshold slope than the physical limit of conventional MOSFET. With the scaling of device dimension, random variability emerges as an important concern and may hinder the feasibility of TFET. The impacts of variations on TFET have been assessed for logic and memory circuits [2-4]. The influence of variability on TFET analog FOM, however, has rarely been known and merits investigation. In this work, using atomistic 3-D TCAD simulations [5], we examine the impact of WFV on TFET analog FOM, and compare our results with the FinFET counterparts.

II. Simulation Methodology

For TFET simulations, the non-local band-to-band tunneling model [5] that accounts for arbitrary tunneling barrier with adequate calibration [6] (A_{path} = 3E17 $cm^{-3}s^{-1}$ and B_{path} = 1.2E7 Vcm^{-1}) is employed. In addition, we have calibrated our mobility model including velocity saturation with the measured data [7] to accurately describe the analog behavior of FinFET. For fair comparison, the TFET and FinFET devices are designed with similar structure (listed in Fig. 1) and comparable off-current (I_{OFF}) (Fig. 2).

In this work, WFV resulting from the poly-grain characteristic of metal-gate material is considered as the main contributing variation source. The Voronoi method [8] that can faithfully imitate the irregular grain patterns is applied with TiN metal-gate material (two distinct orientations with 60% and 40% occurring probability and work function difference of 0.2 eV) and with averaged grain size = 5 nm (see Table I). 3-D Monte Carlo simulations with 150 device samples are carried out to capture the statistical behavior of analog FOMs for TFET and FinFET.

III. Result and Discussion

Fig. 3 shows the impacts of WFV on the I_D-V_G characteristics for TFET and FinFET devices at V_{DS} = 0.6 V. Because of its steeper subthreshold slope, TFET exhibits smaller V_T and slightly larger I_D variation at lower V_G. Fig. 4 shows the comparisons of transconductance (g_m) and g_m/I_D for FinFET and TFET at various gate overdrive (V_{GT}). As can be seen, FinFET exhibits larger g_m and comparable g_m/I_D as compared with TFET at higher V_{GT}. In addition, it is observed that due to the mobility degradation, FinFET suffers significant g_m degradation in the high V_{GT} region. In Fig. 5 and Fig. 6, we compare the normalized g_m and g_m/I_D variations for FinFET and TFET at V_{GT} = 0.2 V and V_{DS} = 0.6 V. In the presence of WFV, FinFET shows comparable normalized g_m and broader g_m/I_D distribution (larger σ/μ) as compared with the TFET counterparts.

Fig. 7 compares the output resistance (R_{out}) for TFET and FinFET. Due to the terminating of drain field in the drain/channel junction (Fig. 7(c)), the tunneling current of TFET arising from the source/channel junction is insensitive to V_{DS} and thus exhibits significantly larger R_{out} than that in FinFET. For FinFET, the drain-induced barrier lowering (DIBL) results in degraded R_{out}. In addition, Fig. 7(d) compares the impacts of V_{GT} on R_{out} for FinFET and TFET. Fig. 8 shows the normalized R_{out} distributions caused by WFV for FinFET and TFET and the corresponding metal-gate grain patterns for the maximum R_{out} of FinFET and TFET. Compared with TFET, FinFET has larger R_{out} variation (larger σ/μ). The intrinsic gain (g_mR_{out}) comparison for FinFET and TFET is shown in Fig. 9. It can be seen that TFET can provide lager gain for V_{GT} below 0.35 V. Fig. 10 compares the intrinsic gain variations of TFET and FinFET at V_{GT} = 0.2 V and V_{DS} = 0.6 V. It is observed that TFET exhibits smaller intrinsic-gain variation (smaller σ/μ) as compared with the FinFET counterparts.

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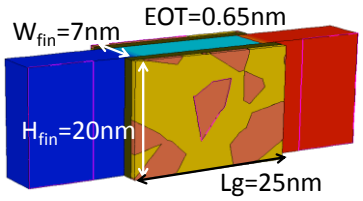

Fig. 1. Schematic of the simulated device structure for FinFET and TFET considering WFV with Voronoi grain pattern [8].

TABLE I. Pertinent parameters used in this work.

Doping Concentration (TFET) (p-i-n)			
Source	3E20 cm^{-3}	Drain	1E20 cm^{-3}
Doping Concentration (FinFET)			
Source	1E20 cm^{-3}	Drain	1E20 cm^{-3}
WFV Simulation			
Workfunction		**FinFET**	**TFET**
WF1 <200> (60%)		4.83 eV	4.26 eV
WF2 <111> (40%)		4.63 eV	4.06 eV

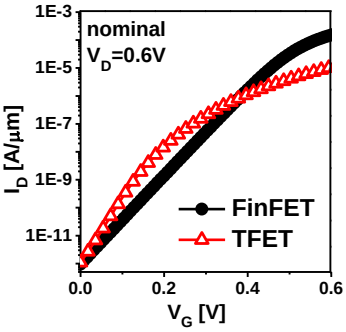

Fig. 2. I_D-V_G of nominal FinFET and TFET. The FinFET and TFET are designed with similar device geometries and I_{OFF}. The V_T value is 0.33 V for FinFET and 0.27 V for TFET determined by constant current 10^{-7} A/um.

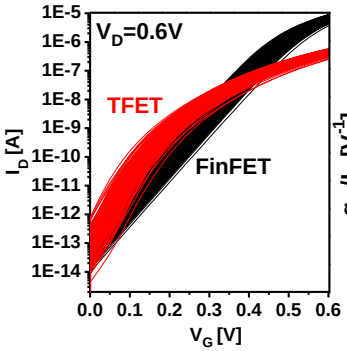

Fig. 3. I_D-V_G dispersions for FinFET and TFET considering WFV. The number of samples is 150.

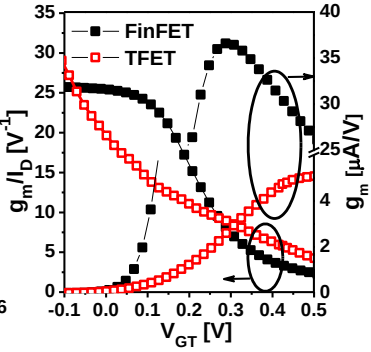

Fig. 4. Comparisons of transconductance (g_m) and g_m/I_D for FinFET and TFET at various V_{GT}.

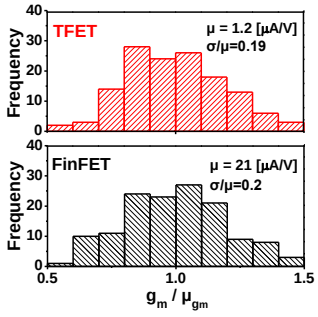

Fig. 5. Comparison of g_m variations for FinFET and TFET at V_{GT} = 0.2 V and V_D = 0.6 V.

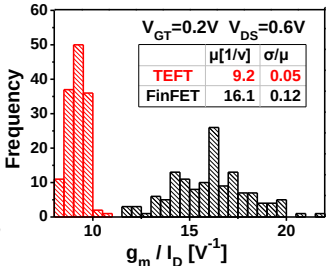

Fig. 6. Comparison of g_m/I_D variations for FinFET and TFET at V_{GT} = 0.2 V.

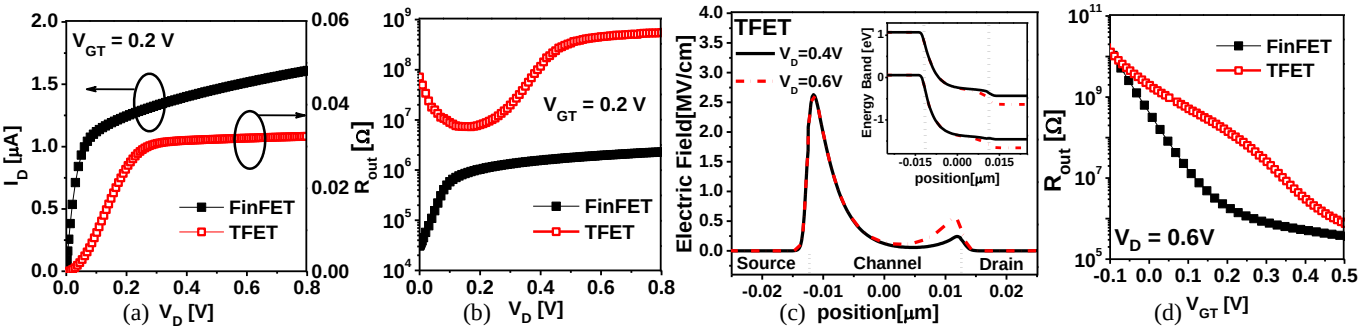

Fig. 7. Comparisons of (a) I_D-V_D and (b) output resistance (R_{out}) for FinFET and TFET at V_{GT} = 0.2 V. (c) Comparisons of electric field and band diagrams (inset) for TFET at V_D = 0.4 and 0.6 V. Fig. 7(d) shows the dependences of R_{out} on V_{GT}.

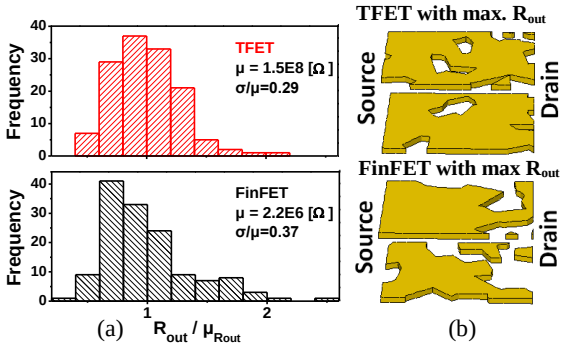

Fig. 8. (a) Comparison of normalized R_{out} variations for FinFET and TFET at V_{GT} = 0.2 V and V_D = 0.6 V and (b) the grain patterns illustrating the maximum R_{out} for FinFET and TFET.

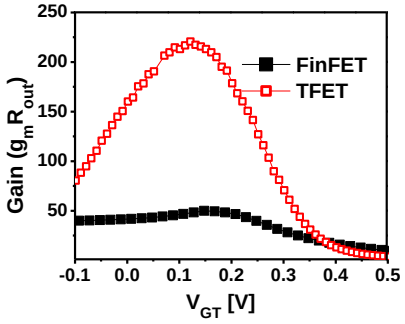

Fig. 9. Intrinsic gain (g_mR_{out}) comparison for FinFET and TFET at V_D = 0.6 V.

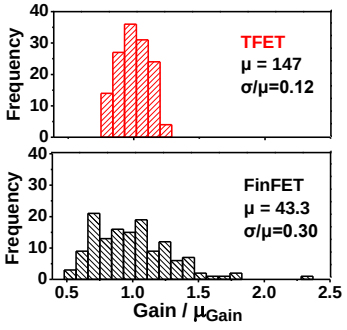

Fig. 10. Distributions of normalized intrinsic gain for FinFET and TFET considering WFV.