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Scalable La-silicate Gate Dielectric on InGaAs Substrate with High Thermal Stability and Low Interface State Density

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1. Introduction

InGaAs is considered as one of the most promising candidates among III-V family to enhance *n*-channel metal-oxide-semiconductor field effect transistors (MOSFETs) performance because of its high electron mobility and manageable band gap with In-content controllability [1]. Significant progress has been made in the recent years, for improving high-k/InGaAs interface, however thermal stability and scaling of these stacks remain a challenge since most of the research is focused on Al_2O_3/InGaAs interface. Diffusion of substrate elements into the dielectric thus degrading its qualities and the formation of low-k interfacial layer as a result of high annealing temperature are some of the issues that face particularly gate first processes where temperatures above 600 ^oC are required for source-drain dopant activation [2].

Recently we reported on La_2O_3/InGaAs interface properties and proposed controlling the diffusion of oxygen from the gate metal to achieve low interface state density (D_{it}) [3]. La-silicate is an amorphous material with high *k*-value which is formed by intermixing of Si and La_2O_3. The *k*-value depends on the Si and La atoms ratio in the final silicate composition [4]. Therefore, application of this material as a gate dielectric to InGaAs can help with scaling and thermal stability of InGaAs-based gate stacks, provided that the silicate/InGaAs interface is carefully controlled.

In this study, methodology for fabricating highly scalable and thermally stable La-silicate layer as a gate dielectric for InGaAs-based MOS capacitors has been investigated.

2. Experimental details

Capacitors were fabricated on S-doped (2×10^{16} cm^{-3}) *n*-$In_{0.53}Ga_{0.47}As$ epiaxially grown on InP substrate. Substrates were treated with HF and $(NH_4)_2S$ at room temperature for oxide removal and surface passivation. 1 nm Si layer was deposited by RF sputtering. Then the substrates' temperature was raised to 200 ^oC and nitrogen radical gun was used to preform nitridation for 5 min, with an estimated total nitrogen doze of 1.5×10^{15} atoms/cm^2. La_2O_3 films were in-situ deposited by e-beam evaporation, followed by RF sputtering deposition of TiN (45 nm)/ W (5 nm) for gate electrodes. Post-metallization anneals (PMA) were carried out in forming gas (FG)(N_2:H_2= 97:3%) ambient for 5 min. Process flow is summarized in Fig. 2. CET of the capacitors was extracted by fitting the 100 kHz C-V curve to the ideal curve calculated for InGaAs band structure. [5]

3. Results and discussion

Fig. 3 and 4 show the effect of initial Si layer thickness on CET and D_{it} of capacitors, respectively. The highest CET stability against PMA temperature and lowest D_{it} was achieved for initial Si thickness of 1 nm. Cross-sectional TEM image of TiN (45 nm)/W (5 nm)/ La_2O_3 (5 nm)/nitridated-Si (1 nm)/InGaAs MOS capacitor after PMA at 520 ^oC in FG is shown in Fig. 3. The reaction of La_2O_3 and nitridated-Si has resulted in a bilayer dielectric layer La_2O_3 (3.5 nm)/LaSiON (1.5 nm) with an effective *k*-value of 24. EDX analysis show the composition of the bottom layer to be consistent of Si, La and elements from the substrate, the top layer on the other hand is mainly composed of La_2O_3. The 100 kHz C-V curves for the La_2O_3 (3.5 nm)/LaSiON (1.5 nm) sample at PMA up to 620 ^oC (Fig. 6) shows healthy C-V characteristics even at high temperatures with CET= 0.6 nm at 620 ^oC. The dependence of La_2O_3/LaSiON stack on deposited La_2O_3 thickness and annealing temperature is shown in Fig. 7. Higher annealing temperature leads to lower CET value, regardless of the initial La_2O_3 thickness. Changes in the composition of LaSiON layer or crystallization of La_2O_3 layer which might occur at high annealing temperatures, could be contributing factors for these results. Although no signs of crystallization were observed at an annealing temperature of up to 520 ^oC from the TEM image. Increasing the PMA temperature is also effective for reducing the D_{it} at LaSiON/InGaAs interface as illustrated in Fig. 9. The interface quality is preserved with La_2O_3 thickness scaling. The gate leakage current of capacitors compared to recently published results is shown in Fig. 10.

4. Summary

InGaAs MOS capacitors with minimum CET of 0.6 nm, thermally stable up to 620 ^oC, with low gate leakage current and D_{it} were fabricated by using amorphous La-silicate structure with effective *k*-value of ~24 as gate dielectric.

Acknowledgements

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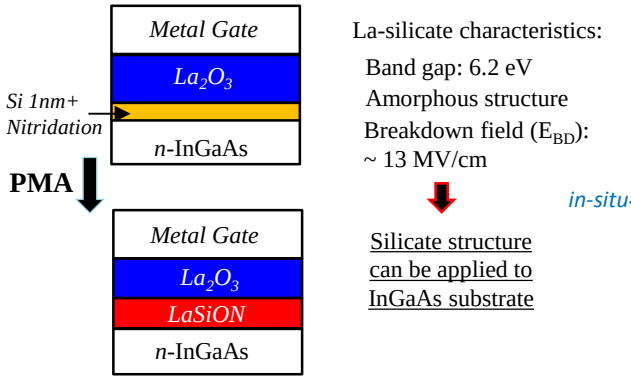


Fig. 1 Schematic of MOS capacitors with La-silicate structure formed by annealing La_2O_3/Si/InGaAs structure

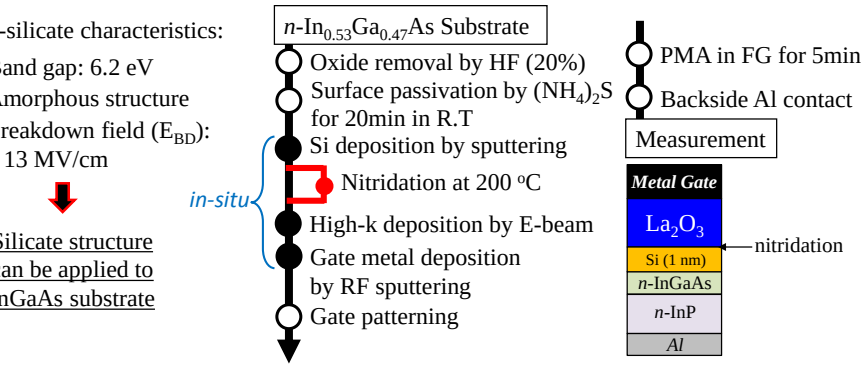


Fig. 2 Device fabrication process for InGaAs MOS capacitors with Si or nitridated-Si at La_2O_3/InGaAs interface

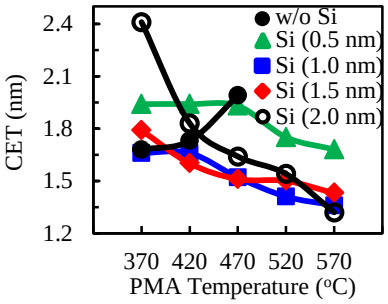


Fig. 3 Si thickness and CET relationship

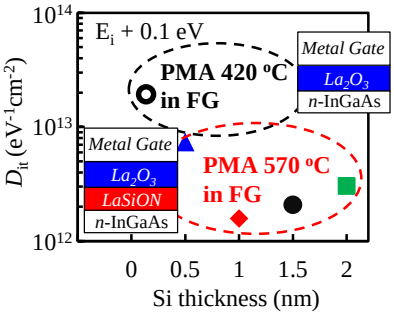
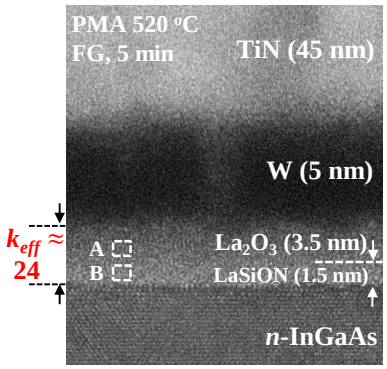


Fig. 4 D_{it} and Si thickness relationship



at. %	In	Ga	As	La	O	Si
A	0.5	0.5	0.5	35	57	7
B	5.2	5.6	7	31	43	8.2

Fig. 5 TEM image of La_2O_3 (5 nm)/nitridated Si (1 nm)/InGaAs interface after 520 °C PMA. EDX of points A and B are shown in the table.

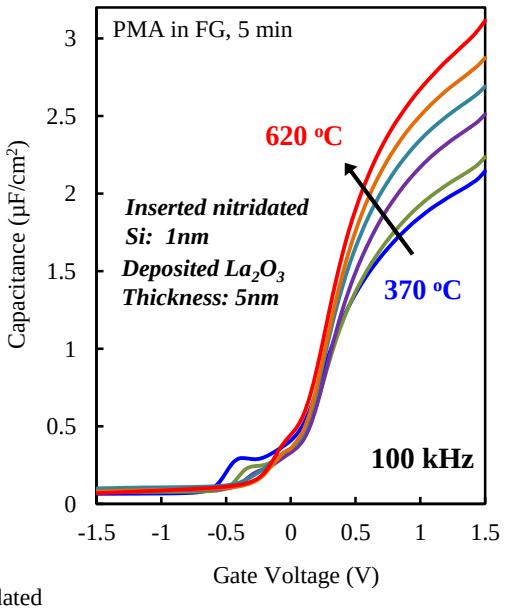


Fig. 6 PMA temperature effect on *CV* characteristics of La_2O_3/LaSiON/InGaAs

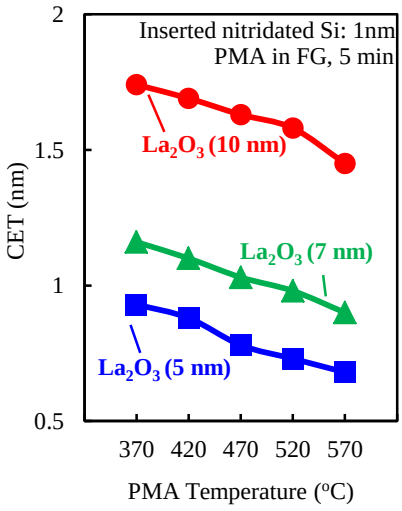


Fig. 7 La_2O_3 thickness effect on CET of capacitors at various PMA

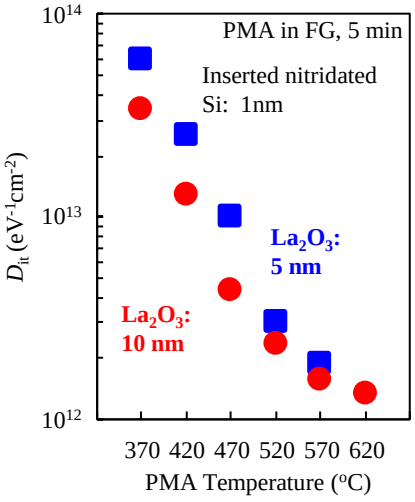


Fig.8 PMA temperature effect on interface State density of La_2O_3/LaSiON/InGaAs

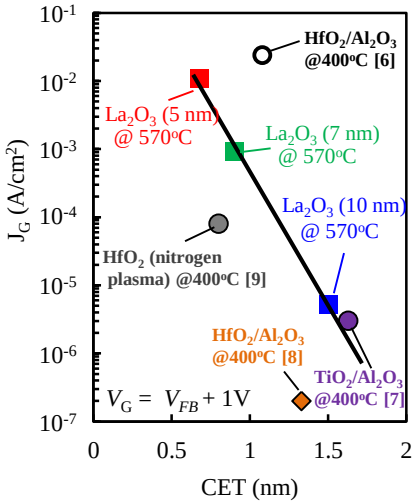


Fig.9 Gate leakage current comparison of La_2O_3/LaSiON/InGaAs