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Channel Length Scaling Limits of III-V Channel MOSFETs Governed by Source-Drain Direct Tunneling

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1. Introduction

Previous experimental [1] and simulation [2-4] studies on Si-MOSFETs found that for channel lengths of less than 6–8 nm, the subthreshold swing becomes drastically worse due to source-drain direct tunneling (SDT). Numerical studies [3,4] also demonstrated that quantum reflection due to a steep potential variation inside the channel leads to a reduction in the on-state drain current. Therefore, there are concerns that the performance of III-V channel MOSFETs with a lower effective mass and enhanced quasi-ballistic transport may be degraded due to such enhanced quantum transport effects, even in devices with longer channels than those used in Si-MOSFETs. In this study, we investigate the influence of quantum transport effects in ultrashort-channel III-V MOSFETs based on a comparison between Wigner Monte Carlo (WMC) simulations [3,4], in which both quantum transport and carrier scattering effects can be fully incorporated, and Boltzmann Monte Carlo (BMC) simulations ignoring quantum transport effects.

2. Device Structure

Fig. 1 shows the device structure. The channel, source and drain materials were InP or $In_{0.53}Ga_{0.47}As$, and their band parameters are summarized in Table I. As is well known, in the Γ valley, $In_{0.53}Ga_{0.47}As$ has a significantly lower effective mass than that for InP and those for Si in the X valley, while it has a larger nonparabolicity in the Γ valley. The electrical characteristics were calculated using the WMC and BMC simulators [4,5], where acoustic phonons, non-polar and polar optical phonons, and impurity scatterings were taken into account.

3. Electrical Characteristics

First, we discuss the electrical characteristics of InP-MOSFETs. Fig. 2 shows the I_D-V_G characteristics for L_{ch} = (a) 30, (b) 15, and (c) 10 nm. It is found that both sets of MC results are almost identical for L_{ch} = 30 nm. However, for $L_{ch} \leq 15$ nm, the subthreshold current determined by the WMC simulation rapidly becomes larger than that by the BMC simulation. This is due to SDT, as will be shown later. It should also be noted that the drain current at high gate voltages is almost the same for both simulations, regardless of L_{ch}. This implies that quantum reflection has a negligible influence on the on-state drive current.

Figs. 3 and 4 show the distribution functions for $V_G = V_{th}$ and V_{on}, respectively, for L_{ch} = (a) 30 and (b) 10 nm. From Fig. 3(a), it is found that the two distribution functions are remarkably similar not only in the source and drain regions but also in the channel region, indicating that SDT is almost negligible for L_{ch} = 30 nm. On the other hand, for L_{ch} = 10 nm, an interference pattern is observed in the Wigner distribution function inside the channel, as shown in Fig. 3(b). Since this is a signature of tunneling [3,4], SDT is actually taking place. As seen in Fig. 4, for $V_G = V_{on}$, there are only slight differences between the WMC and BMC distribution functions for either L_{ch}, since the main current is governed by classical thermal electron emission at the source-channel junction. Unlike the case for Si-MOSFETs, quantum reflection is almost negligible, and thus the on-state current reduction is hardly observed as shown in Fig. 2 [5].

Next, Fig. 5 shows the I_D-V_G characteristics computed for InGaAs-MOSFETs. The subthreshold current increase due to SDT is more remarkable than in the InP-MOSFETs. Then, threshold current increase due to SDT with reducing L_{ch} is compared between the two III-V materials, as shown in Fig. 6. It is found that the influence of SDT becomes evident for $L_{ch} < 20$ nm, for both III-V materials. We confirmed that the critical channel lengths are independent of T_{ox}. As expected, the InGaAs-MOSFETs exhibit larger subthreshold current increase, but the difference from the InP counterpart is quite smaller than one expected from the significant difference in the effective masses. We consider it due to the fact that the channel potential profile at $V_G = V_{th}$ is substantially different between the two channel materials, as shown in Fig. 7. In other words, InGaAs-MOSFET produces a higher potential barrier than in InP-MOSFET due to the larger band nonparabolicity in the Γ valley, which might work to suppress SDT. Here, it should also be noted that the critical channel length indicated above is approximately three times larger than that for Si-MOSFETs, plotted as dashed line in Fig. 6 [2]. Therefore, countermeasures should be taken to suppress SDT in order to aggressively downscale III-V MOSFETs. One approach may be the choice of a material with a higher transport mass, or to be more precise, a higher tunneling mass. Higher mass materials would also help to reduce the DOS bottleneck problem in quantum capacitance limit [5].

4. Conclusions

It was found that SDT becomes evident for $L_{ch} < 20$ nm in III-V MOSFETs. On the other hand, quantum reflection was shown to have a negligible effect on the on-state drain current. It will be necessary to develop measures for suppressing SDT before Si-MOSFETs can be replaced.

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References [1] H. Kawaura et al., *APL* **76** (2000) 3810. [2] Y. Yamada et al., *IEEE-TED* **56** (2009) 1396. [3] D. Querlioz et al., *IEEE-TED* **54** (2007) 2232. [4] S. Koba et al., *SISPAD 2011*, pp. 79-82. [5] S. Koba et al., *APEX* **6** (2013) 064301.

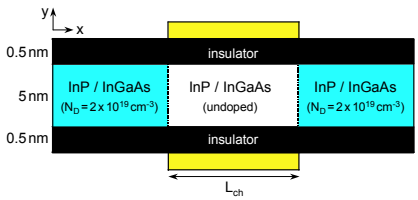


Fig. 1 Device structure. A double-gate structure was employed with a channel thickness of 5 nm and a SiO_2 gate oxide thickness (T_{ox}) of 0.5 nm. The source and drain donor concentration is 2×10^{19} cm^{-3}.

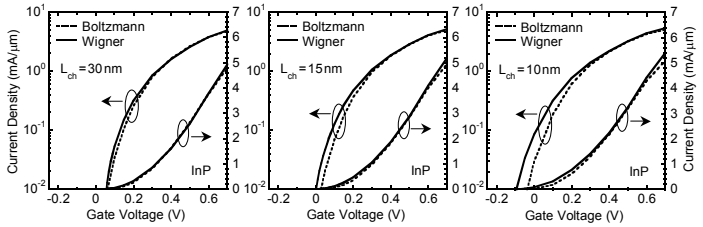


Fig. 2 I_D-V_G characteristics of InP-MOSFETs computed at V_D = 0.5 V for L_{ch} = (a) 30, (b) 15, and (c) 10 nm, where the WMC and BMC results are plotted as solid and dashed lines, respectively.

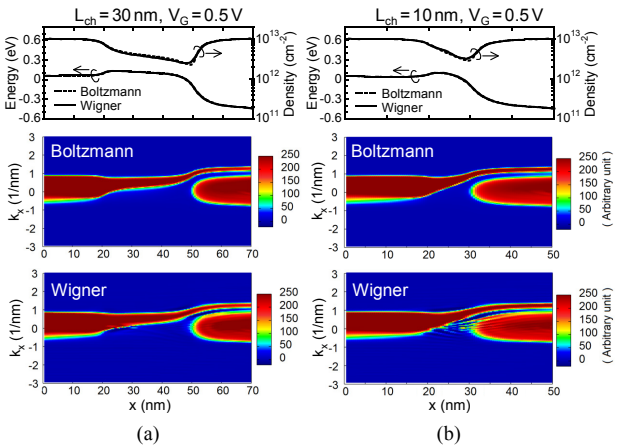


Fig. 4 Computed phase-space distribution functions of InP-MOSFETs for L_{ch} = (a) 30 and (b) 10 nm at an on-state gate voltage V_{on}, defined as the gate voltage corresponding to I_D = 3 mA/μm from the BMC simulations. Note that the sheet electron density distributions calculated using the two MC methods are almost identical, regardless of L_{ch}.

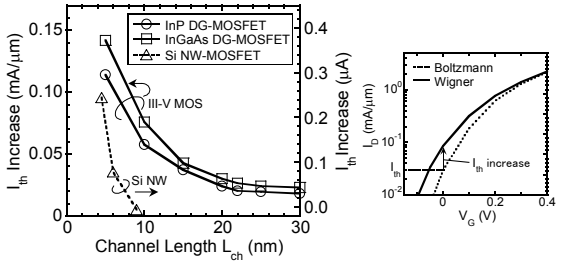


Fig. 6 L_{ch} dependence of I_{th} increase due to SDT. The result for GAA-Si nanowire MOSFETs [2] is also plotted for comparison. The right panel shows the method used to calculate the I_{th} increase.

Table I. Band parameters used in the simulation, with the values for Si included. In the simulations, only the Γ and L valleys were considered, since $\Delta E_{\Gamma X}$ is significantly larger than the increase in kinetic energy of electrons due to the supply voltage provided.

		Si	InP	$In_{0.53}Ga_{0.47}As$
mass (Γ)		–	0.082	0.046
mass (X)	m_t (m_0)	0.19	0.273	0.251
	m_l (m_0)	0.98	1.321	2.852
mass (L)	m_t (m_0)	0.126	0.153	0.125
	m_l (m_0)	1.634	1.878	1.552
nonparabolicity α (eV^{-1})		0.5 (X) 0.3 (L)	0.61 (Γ) 0.49 (L) 0.12 (X)	1.18 (Γ) 0.43 (L) 0.33 (X)
ΔE_{XL} (eV)		1.049	–	–
$\Delta E_{\Gamma L}$ / $\Delta E_{\Gamma X}$ (eV)		–	0.832 / 1.492	0.723 / 1.062
band gap (eV)		1.12	1.34	0.86
permittivity ε_r		11.9	12.6	14.1

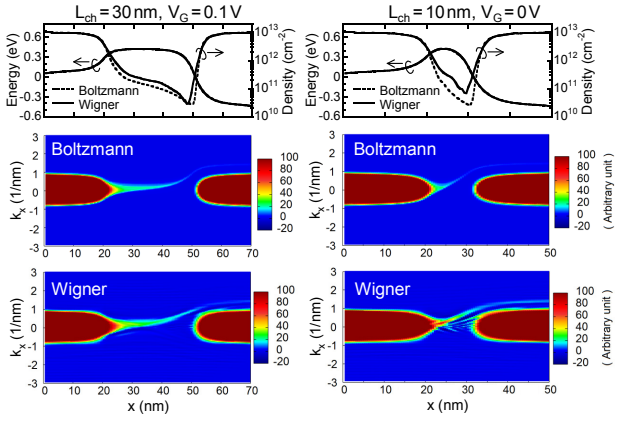


Fig. 3 Computed phase-space distribution functions of InP-MOSFETs for L_{ch} = (a) 30 and (b) 10 nm at a threshold gate voltage V_{th}, defined as the gate voltage corresponding to I_D = 0.03 mA/μm from the BMC simulations. The upper panels show the spatial distributions of the lowest-subband energy in the Γ valley and the total sheet electron density. SDT in L_{ch} = 10 nm is also confirmed by the significant increase in the channel sheet density observed in the WMC results.

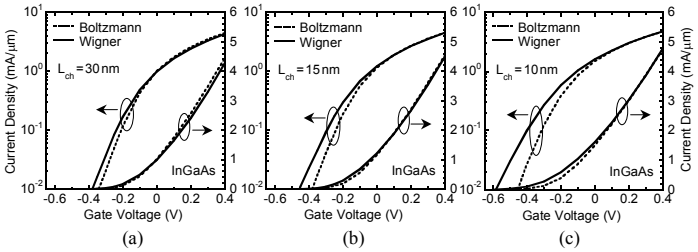
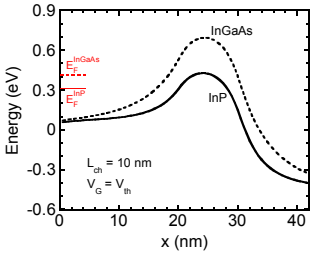


Fig. 5 I_D-V_G characteristics of InGaAs-MOSFETs computed at V_D = 0.5 V for L_{ch} = (a) 30, (b) 15, and (c) 10 nm.



Channel barrier height measured from E_F is higher in InGaAs-MOSFETs compared to InP-MOSFETs due to the larger band nonparabolicity in Γ valley, which makes density-of-states larger as electron energy becomes higher.

Fig. 7 Spatial distributions of the lowest-subband energy in the Γ valley at V_G = V_{th}. Since the strength of SDT is determined by channel length, carrier effective mass and also barrier height, higher potential barrier in InGaAs-MOSFET might work to suppress SDT.