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Effect of Alloy Scattering on Hole Mobility of sSi/sSiGe/sSOI Quantum Well pMOSFETs

Wangran Wu[1], Wenjie Yu[2], Qingtai Zhao[3], Jiabao Sun[1], Dongyuan Zhai[1], Yi Shi[1], and Yi Zhao[*1, 4]

[1]School of Electronic Science and Engineering, Nanjing UniversityNanjing 210093, People's Republic of China
* E-mail: yzhao@nju.edu.cn
[2]State Key Laboratory of Functional Materials for Informatics, Shanghai, 200050, People's Republic of China
[3]Peter Grünberg Institute 9 (PGI 9-IT), Forschungszentrum Juelich, 52425 Juelich, Germany
[4]State Key Lab of Silicon Materials, Zhejiang University, Hangzhou 310027, People's Republic of China

1. Introduction

Much attention has been paid to $Si/Si_{1-x}Ge_x$ quantum well (QW) pMOSFET because of its high hole mobility and the compatible process with the existing sophisticated Si technology [1]. The key idea of high mobility QW pMOSFETs is to exploit the effects of strain and confinement to reduce the carrier effective mass and scattering rate, resulting in the mobility improvement. Meanwhile, in order to realize a good gate dielectric/Si interface, a thin Si cap layer with a thickness of about 3nm is needed to avoid the hole mobility degradation [2]. Several possible factors, including the gate dielectric/Si cap stack, strain level and carriers scattering mechanisms, are being considered to affect the hole mobility. In terms of the carriers scattering mechanisms, beside the conventional ones (Coulomb scattering, surface roughness scattering and phonon scattering) in the MOSFETs devices, the alloy disorder scattering in $Si_{1-x}Ge_x$ could also be another possible issue we have to take into consideration for QW pMOSFET. However, it is theoretically contentious that whether the alloy scattering in $Si_{1-x}Ge_x$ could significantly degrade the carriers mobility [3-4]. On the other hand, the direct experimental investigation of the alloy scattering is difficult because of the existence of other scattering mechanisms. Thus, it is still experimentally unclear that to what extend does the alloy scatting in the $Si_{1-x}Ge_x$ channel remove the gains brought by the reduced effective mass considering the overall hole mobility.

In this study, we experimentally investigate the mobility limited by alloy scattering (μ_{alloy}) of QW pMOSFETs through varying the back-gate bias (V_{back}) and low temperature mobility analysis. It is found that the negative back-gate bias could cause the decrease in the hole mobility of QW pMOSFET, which is opposite to the case of traditional SOI MOSFETs [5]. It is experimentally confirmed that this mobility decrease could be attributable to the alloy scattering in the $Si_{1-x}Ge_x$ channel.

2. Experimental

Figure 1(a) shows the transmission electron microscope (TEM) image of the $sSi/Si_{0.5}Ge_{0.5}/sSOI$ heterostructure substrate prepared for the transistor fabrication. A 25nm thick $Si_{0.5}Ge_{0.5}$ layer was grown on a lightly p-doped bi-axially tensile (ε =0.8%) strained SOI with a thickness of 12nm. Then the Si cap layer with a thickness of 5nm (before annealing) is deposited on the substrate. The schematic view of the QW pMOSFETs, fabricated by a standard a gate-first device process, is shown in Fig. 1(b). Hole mobility was extracted by the split C-V method under both room temperature and low temperature, during which various back-gate biases were applied to modulate the hole distribution in the $Si_{0.5}Ge_{0.5}$ channel.

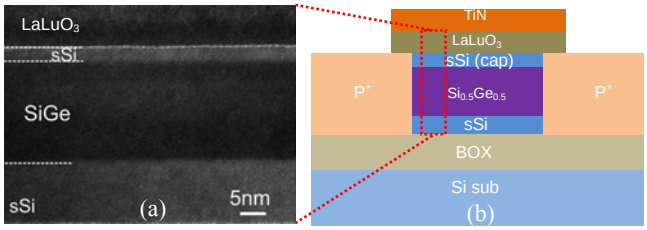

Fig. 1 (a)TEM images of the $sSi/Si_{0.5}Ge_{0.5}/sSOI$ substrate after S/D annealing; (b)Schematic view of the $sSi/Si_{0.5}Ge_{0.5}/sSOI$ QW pMOSFET with $LaLuO_3$ as gate stacks.

3. Results and discussion

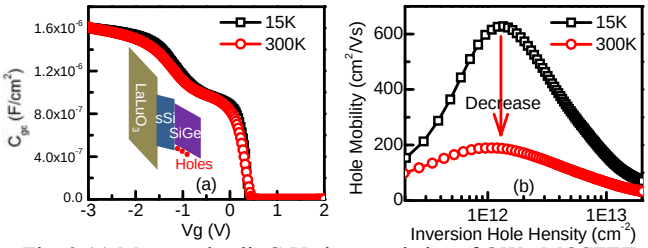

Fig. 2 (a) Measured split C-V characteristics of QW pMOSFET at 15K and 300K after correction of the overlap capacitance; (b) Measured Hole mobility of the QW pMOSFETs at 15K and 300K.

The split C-V curves of the QW pMOSFET present typical dual channel characteristics [Fig. 2(a)]. When the gate voltage is about 1V, as shown in the inset of Fig. 2(a), holes are confined in the $Si_{0.5}Ge_{0.5}$ QW well formed by the large valence band offset at the $sSi/Si_{0.5}Ge_{0.5}$ interface. The mobility data [Fig. 2(b)] shows that the peak hole mobility (when the inversion hole density, N_s, is about 10^{12} cm^{-2}) at room temperature is much smaller than that at low temperature. Since the Coulomb scattering is relatively weak at room temperature when N_s is large and continuous decrease with the increase in N_s because of the screening effect [6], therefore, it is likely that the obvious peak mobility decrease at room temperature, compared with that at low temperature, is due to the phonon scattering and alloy scattering.

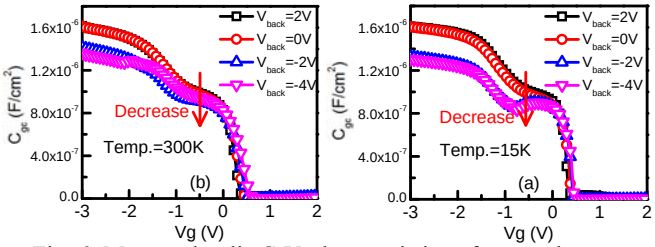

Fig. 3 Measured split C-V characteristics after overlap capacitance correction of QW pMOSFET under various back-gate biases at (a) 300K and (b) 15K.

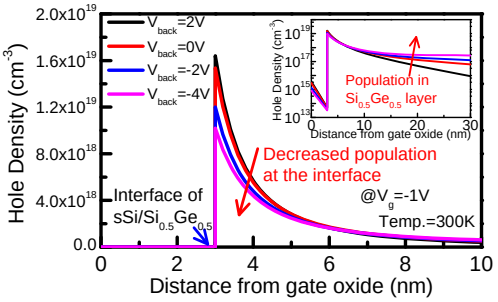

Fig. 4 Simulated hole distribution in the QW pMOSFET when V_g=1V at 300K under various back-gate biases through Medici.

In order to verify the impact of alloy scattering in the $Si_{0.5}Ge_{0.5}$ channel, various back-gate biases were applied to modulate the holes distribution during the split C-V and mobility test. Figure 3 shows the split C-V curves under different back-gate biases at both 300K and 15K. After the QW channel formed (the first step of the C-V curve), the capacitance decreases under the negative back-gate bias, which means that holes populated farther away from the gate oxide. Also, the simulated results carried out by Medici (Fig. 4) indicate that the applied negative back-gate biases would decrease the population of holes close to the interface of sSi/$Si_{0.5}Ge_{0.5}$ and increase the holes population in the $Si_{0.5}Ge_{0.5}$ layer away from the sSi cap.

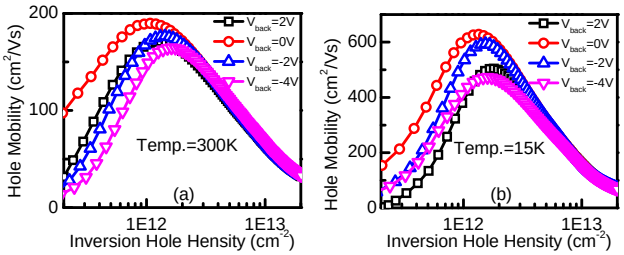

Fig. 5 Measured hole mobility of the QW pMOSFET under various back-gate biases at (a) 300K and (b) 15K.

From the measured hole mobility (Fig. 5), we can see that both positive and negative back-gate biases could decrease the hole mobility in the low field region, which is different from the case of normal SOI pMOSFETs. In normal SOI pMOSFETs, the negative back-gate bias increases the mobility in the low field region because the carriers distribute further from the gate oxide/channel interface, resulting in less Coulomb scattering from the interface states [5]. However, in the QW pMOSFETs, when the back gate is negatively biased, more holes distribute in the $Si_{0.5}Ge_{0.5}$ layer and that would cause more severe alloy scattering, which leads to the mobility decrease.

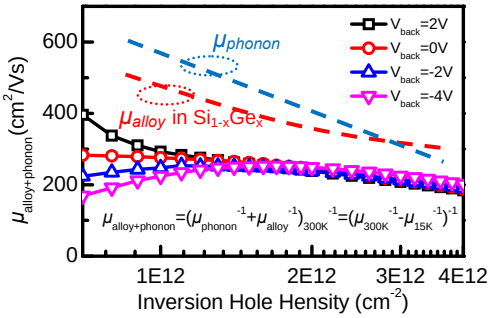

Fig. 6 $\mu_{alloy+phonon}$ versus the inversion hole density under different back-gate biases obtained from the measured hole mobility at 300K and 15K.

Since the mobility begins to decrease when N_s is larger than about 10^{12} cm^{-2}, Coulomb scattering would not be the major factor because of screening effect in this region [6]. Meanwhile, because the phonon scattering would vanish at 15K [6] and μ_{alloy} at 15K is much higher than that at 300K [4], we could obtain $\mu_{alloy+phonon}$ from the measured hole mobility at 300K and 15K through the relationship shown in Fig. 6. As shown in Fig. 6, with a zero or negative V_{back}, the alloy scattering is more pronounced than phonon scattering when N_s is smaller than 10^{12} cm^{-2} otherwise $\mu_{alloy+phonon}$ under negative biases should be higher because of the higher μ_{phonon} in $Si_{0.5}Ge_{0.5}$ [3]. When V_{back} is -4V, $\mu_{alloy+phonon}$ increases slowly with N_s due to the decrease in alloy scattering caused by the holes population closer to the interface as V_g decreases. Both μ_{alloy} and μ_{phonon} decrease with the increase in N_s and finally μ_{alloy} surpasses μ_{phonon} in the high N_s region.

4. Conclusions

We have extensively investigated the alloy scattering in the QW pMOSFET with a sSi/$Si_{0.5}Ge_{0.5}$/sSOI substrate by modulating the hole distribution through applying back-gate biases. The applied negative back-gate bias would cause the decrease in the hole mobility because of the enhancement of the alloy scattering in $Si_{0.5}Ge_{0.5}$ layer. Furthermore, the alloy scattering is more pronounced than phonon scattering when N_s is smaller than 10^{12} cm^{-2} and inferior to phonon scattering in the high N_s region. The results should be important for further understanding the scattering mechanisms in $Si_{1-x}Ge_x$ QW MOSFETs and enhancing the device performances.

Acknowledgements

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