

## Understandings on Surface Orientation Impacts on Random Telegraph Signal Noise Related Carriers Trapping Time Constants and Current Fluctuations

Jiezhi Chen, Izumi Hirano, and Yuichiro Mitani

Advanced LSI Technology Laboratory, Corporate Research & Development Center, Toshiba Corporation

1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210-8582, Japan

Tel: +81-44-549-2188, Fax: +81-44-520-1804, Email: chen.jiezhi@toshiba.co.jp

### Abstract

Random telegraph signal (RTS) noise in (110)- and (100)-orientated nMOSFETs are studied systematically, with main focuses on surface orientation impacts on carrier trapping time constants and traps induced channel current fluctuations. On the one side, single trap's RTS noise and multiple traps' RTS noise are all evaluated to estimate current fluctuations ( $\Delta I_d/I_d$ ) and threshold voltage shifts ( $\Delta V_{th}$ ). It is observed that  $\Delta I_d/I_d$  and  $\Delta V_{th}$  degradations are much more serious in (110) nFETs. On the other side, couplings between time constants and applied gate biases are compared. Traps in (110) nFETs illustrate much stronger couplings than in (100) nFETs, which might related to various trap positions and inversion electron distributions. Correlations between current fluctuations and couplings are also discussed for further understandings.

### Introduction

Along with development of scaling-down techniques, device structures are changed from traditional flat structures to three dimensional (3D) structures. Accordingly, in order to improve device performances with higher carrier mobility and steeper sub-threshold slopes, structure optimizations have been studied systematically [1]. Simultaneously, how to suppress reliability degradation in small area devices, like worse RTS noise, is also important. Studies on RTS noise have been continued for a long time and intensively reported in last few years because its serious impacts in scaling-down devices and circuits can not be ignored anymore, such as CMOS image sensors [2] and NAND flash memories [3]. Accordingly, finding acceptable balances between performances and reliabilities by optimizing structures is believed to be critical from now on.

It was used to be reported that performances in (110) nFETs are approaching to those in (100) nFETs as scaling down [4], while experiment work on RTS noise comparison between (110) and (100) devices are still limited [5]. In this work, impacts of surface orientations on RTS noise are systematically studied in both (100) nFETs and (110) nFETs, including trap time constants and carrier trapping induced fluctuations ( $\Delta I_d/I_d$ ,  $\Delta V_{th}$ ). On the one hand, it is found that couplings between time constants and gate biases are stronger in (110) nFETs; on the other hand,  $\Delta I_d/I_d$  and  $\Delta V_{th}$  degradations are much more serious in (110) FETs. Physical mechanisms on correlations between time constant couplings and fluctuation amplitudes are also discussed for further understandings.

### Experimental Results and Discussions

#### A. RTS noise characterization methods

RTS noise are studied and compared in (110) nFETs and (100) nFETs with identical 2nm gate oxide, by using Agilent B1530 RTS noise characterization system. Channel doping concentration ( $N_{ch}$ ) ranges from  $2E17cm^{-3}$  to  $2E18cm^{-3}$ . Typical RTS phenomena due to one and two traps are illustrated respectively in Fig. 1(a). For single trap, detail information of time constants can be extracted, such as time to capture ( $\tau_c$ ), time to emission ( $\tau_e$ ), and time constant couplings on the gate bias ( $\alpha_{\tau_c}$ ,  $\alpha_{\tau_e}$ ,  $\alpha_{\tau_c/\tau_e}$ ), as shown in Fig. 1(b). For multiple traps, though time constants of each trap are difficult to be extracted, histogram graph of drain currents or time lag plot (PLT) [6] can be utilized to estimate trap numbers as well as  $\Delta I_d/I_d$ . So, surface orientation impacts on trap density can be qualitatively studied.

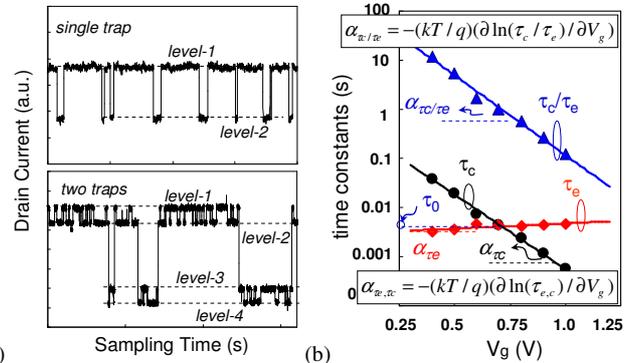


Fig.1 (a) Observation of typical RTS noise, single trap induced two  $I_d$  levels and two traps induced four  $I_d$  levels; (b) extracted time constants from single trap RTS noise,  $\tau_c$ ,  $\tau_e$  and  $\tau_c/\tau_e$ .

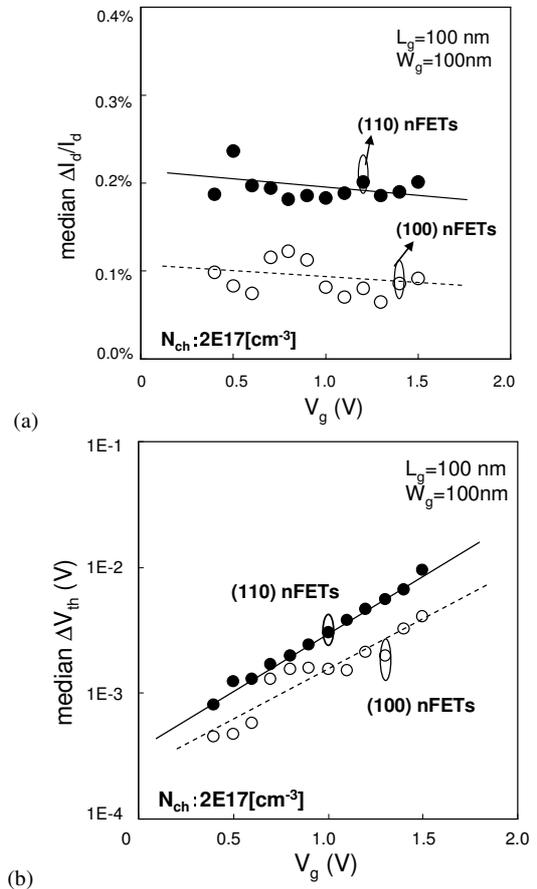


Fig.2 Measured properties of (a)  $\Delta I_d/I_d$  versus  $V_g$ , and (b)  $\Delta V_{th}$  versus  $V_g$ , in (100) nFETs and (110) nFETs. Dotted and solid lines are used as trend lines.

#### B. RTS noise in (100) and (110) nFETs

Firstly, single trap and multiple traps are both evaluated for statistic analysis on RTS noise impacts. Here,  $\Delta V_{th}$  is estimated by using measured  $g_m$  from  $I_d$ - $V_g$  sweeping together with  $\Delta I_d$  from  $I_d$  sampling at a fixed  $V_{g0}$ , via  $\Delta V_{th} = \Delta I_d(V_{g0})/g_m(V_{g0})$ .

Here,  $V_{g0}$  is defined as the applied  $V_g$  at  $\tau_0$  (Fig. 1(b)). Generally, single trap induced  $\Delta I_d/I_d$  fluctuations should be suppressed at higher  $V_g$  because of stronger screening effects. However, as increasing  $V_g$ , traps at higher energy levels will contribute to observed  $\Delta I_d/I_d$ , and average  $\Delta I_d/I_d$  values show weak  $V_g$  dependences. Similarly, considering  $g_m$  degradations at higher  $V_g$ ,  $\Delta V_{th}$  dependences on  $V_g$  (Fig. 2(b)) could be explained. Nevertheless, as shown in Fig. 2, it is found that  $\Delta I_d/I_d$  and  $\Delta V_{th}$  degradations in (110) devices are much more serious than those in (100) devices. Since noise power spectrum density (PSD) is in proportion to the trap density  $N_{it}$  [7], larger fluctuations in (110) nFETs can be explained by worse  $N_{it}$  in SiO<sub>2</sub> on (110) surface. As shown in Fig.3, it is found that RTS trap densities in (110) nFETs are almost twice as many as those in (100) nFETs.

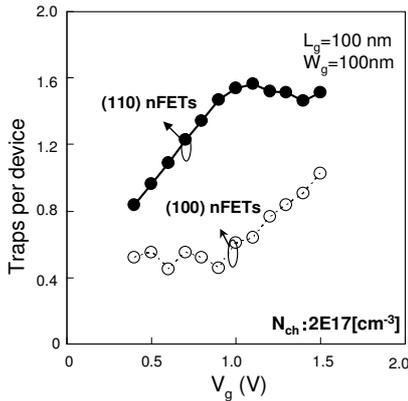


Fig.3  $V_g$  dependences of average trap numbers per device, which are estimated from  $I_d$  fluctuation levels [5, 6].

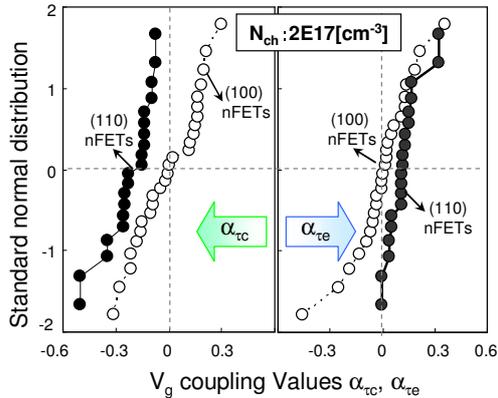


Fig.4 Channel doping dose dependences on time constant couplings to  $V_g$ ,  $\alpha_{tc}$  and  $\alpha_{te}$ . In comparison to (100) nFETs, traps in (110) nFETs illustrates stronger couplings of  $\tau_c$  and  $\tau_e$ .

For more information, couplings of  $\alpha_{tc}$  and  $\alpha_{te}$  are estimated and plotted in Fig.4. Similar to previous work in [8], positive  $\alpha_{tc}$  are difficult to be observed in most cases, except in low channel doping (100) nFETs. Since positive  $\alpha_{tc}$  likely belongs to traps that are closer to the upper interface and they trap/de-trap carriers from/into gate side [9], traps with positive  $\alpha_{tc}$  might be easily screened by traps that locate closer to the lower interface of SiO<sub>2</sub>/Si-sub. Nevertheless, in comparison to traps in (100) nFETs, traps in (110) nFETs show stronger couplings ( $\alpha_{te}$ ,  $\alpha_{tc}$ ). Then,  $\alpha_{tc/\tau_e}$  in (110) nFETs and (100) nFETs are compared in Fig.5 (a). It is interesting to find that,  $\alpha_{tc/\tau_e}$  in (110) nFETs are obviously larger than that in (100) nFETs. In the classical model [6], trap position ( $X_T$ ) and coupling are identical,  $\alpha_{tc/\tau_e} \sim X_T/T_{ox}$ , by supposing carriers locate just at the surface. In fact, inversion carriers should be treated quantum-mechanically with discrete energy levels and distribute with a distance from the surface.

Therefore,  $\alpha_{tc/\tau_e}$  should be expressed as  $(X_T+z_{inv})/T_{ox}$ ,  $z_{inv}$  is the average distance from the surface to electrons. On the one side,  $\alpha_{tc/\tau_e}$  might be related to various trap positions in SiO<sub>2</sub> on (100) and (110) surface [11]. On the other side, it is known that  $z_{inv}$  is inversely proportional to the effective mass  $m_z^*$  of electrons perpendicular to the surface via  $z_{inv} \propto (m_z^*)^{-1/3}$  [10].  $m_z^*$  in (100) surface is  $0.918m_0$  ( $m_0$ : free-electron mass) for the lowest subband while that in (110) surface is  $0.315m_0$ . Deeper  $z_{inv}$  goes with lighter  $m_z^*$ , which means electron distributions in (110) surface are deeper from the surface (Fig. 5(b)). In simple words, deeper  $z_{inv}$  and possible farther  $X_T$  could enhance  $\alpha_{tc/\tau_e}$ .

More importantly, larger  $\alpha_{tc/\tau_e}$  in devices of higher channel doping are observed in both (100) nFETs and (110) nFETs, indicating that substrate dopant fluctuations (RDF) can also strength couplings. These agree with 3D simulation results [12], in which it is believed that electrostatics could be largely modulated by RDF. In other words, various  $\alpha_{tc/\tau_e}$  could also partly originate from different dopant profiles in (110) and (100) substrates. Furthermore, it was used to find that  $\Delta I_d/I_d$  are correlated to coupling values ( $\alpha_{tc/\tau_e}$ ) [8], as what we observed in (110) nFETs. Actually,  $\Delta I_d/I_d$  can be explained by modulations on carrier distributions after carriers' trapping. Larger  $\Delta I_d/I_d$  degradation is possibly triggered by larger  $\Delta z_{inv}$ , which can also enhance  $\alpha_{tc/\tau_e}$  because  $z_{inv}$  should be replaced with  $z_{inv} + \Delta z_{inv}$ . It should be noted that  $\Delta z_{inv}$  is not only determined by traps in the dielectrics, but also by RDF in the substrate. In addition,  $\Delta z_{inv}$  could possibly explain why correlations between trap positions and  $\Delta V_{th}$  are difficult to be experimentally observed [5, 6].

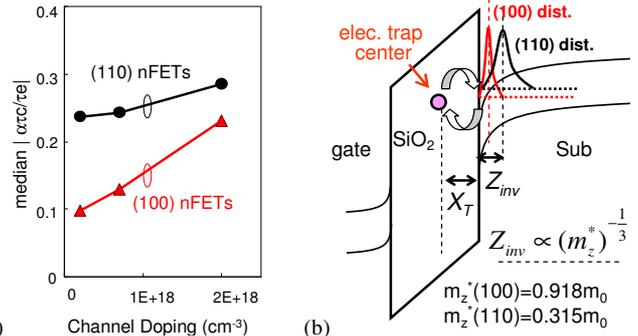


Fig.5 (a) Channel doping dose dependences on  $\alpha_{tc/\tau_e}$ . In comparison to (100) nFETs, (110) nFETs show larger  $\alpha_{tc/\tau_e}$ , which possibly originate from (b)  $z_{inv}$  differences between (110) nFETs and (100) nFETs.

## Conclusions

RTS noise in both (100) and (110) nFETs are characterized and compared systematically. In comparison with (100) nFETs, stronger couplings of time constant to gate biases and larger current fluctuations are observed in (110) nFETs. Wherein, various inversion electron distributions and possible farther trap distributions are considered to be important reasons for larger couplings, while worse trap densities can contribute to larger  $\Delta I_d/I_d$  degradations. Correlations between  $\Delta I_d/I_d$  and couplings are also discussed for further understandings.

(The authors would like to thank Dr. K. Tatsumura for the sample provision, and Dr. Higashi for helpful discussions)

## Reference:

- [1] M. Saitoh *et al.*, VLSI 2008, p.18; [2] M. Gonthier *et al.*, IEDM 2011, p.183; [3] D. Kang *et al.*, VLSI2011, p.206; [4] P. Packan *et al.*, IEDM 2008, p.63; [5] J. Chen *et al.*, VLSI2012, p.141; [6] T. Nagumo *et al.*, IEDM 2009, p.759; [7] K. K. Hung *et al.*, TED, 37(3), p.654; [8] H. Miki *et al.*, VLSI 2011, p.148; [9] L. Zhang *et al.*, VLSI 2009, p.46; [10] Y. Taur *et al.*, Fundamentals of Modern VLSI Devices; [11] Y. Mitani *et al.*, IRPS 2010, p.299; [12] C. M. Compagnoni *et al.* TED, 59(9), p.2459.