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Analyzing the Reliability of High-κ Dielectric Metal Gate MOSFETs by Using Random Telegraph Signal

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1. Introduction

Positive and negative bias temperature instability (P/NBTI) has been recognized as two major reliability issues in advanced CMOSFET systems containing MG/HK dielectrics [1]. On the other hand, one of the most significant reliability issues in advance device scaling is random telegraph signal (RTS) [2~4]. Recent studies have shown charging/discharging of oxide defects induce threshold voltage amplitude distribution in RTS and NBTI [5]. We focus on threshold voltage fluctuations in high-κ (HfO_2) gate dielectric MOSFETs due to threshold voltage random telegraph signal ($V_{th,RTS}$) amplitude distribution under P/NBTI. By using the statistical analysis, the generation of random trap density and the number of the occupied oxide traps can be estimated by numerical calculation, which helps intuitive understanding of RTS impact on the reliability of MG/HK MOSFETs.

2. Experiment

RTS measurement in high-κ (HfO_2) gate dielectric and metal gate MOSFETs are performed with fast and accurate I-V characterization using an Agilent B1530A. The n- and p-MOSFETs have a drawn gate length of 30 nm and a gate width of 200 nm, respectively. The physical thickness of the HfO_2 was 2 nm. The physical thickness of the interfacial layer (IL) was 1.1 nm. The effective oxide thickness in n-MOSFET is 1.18 nm and in p-MOSFET is 1.16 nm, respectively.

3. Results and Discussion

Fig. 1 shows RTS noise in small-area MOSFETs is due to the effect of trap that captures and emits charge carriers in the oxide, leading to the fluctuation of the threshold voltage (V_{th}) between multiple-level corresponding to the multiple charging states of the trap in time domain. We can clearly observe two-level fluctuation in Figs. 2(a), four-level fluctuation in Fig. 2(b) and eight-level fluctuation in Fig. 2(c), respectively. As the trap number (n) increases, the number of level fluctuation increases with 2^n, and $\Delta V_{th,RTS}$ tends to be large [6]. Moreover, the cumulative-distribution-functions (CDF) of $\Delta V_{th,RTS}$ of both the n- and p-MOSFET are shown in Fig. 3 and Fig. 4, respectively. The CDF of $\Delta V_{th,RTS}$ was measured at the drain voltage of 50mV, the gate voltage was set from 0.75V to 0.95V and the step is 0.1V at high temperature (125°C). Fig. 5 shows the location level of the trap in the effective dielectric responsible of RTS between PBTI in n-MOSFET and NBTI in p-MOSFET by the equation (3) and (4).The result shows that $\Delta V_{th,RTS}$ of the p-MOSFET is obviously larger than that of the n-MOSFET. The $\Delta V_{th,RTS}$ between PMOS and NMOS devices can be explained by the difference in the capture cross-section of oxide dielectric.

It is very important to note that RTS is not only a variability issue, but also a long term of reliability issue, similar to P/NBTI. In P/NBTI test, the stress condition are $|V_g - V_t|$ / oxide electric field = 7 MV/cm and V_D = 0 V at high temperature (125°C). After the long time stress (20k sec), $V_{th,RTS}$ are immediately traced with the condition that drain voltage is 50mV, and the gate voltage is adjusted to have a target drain current of 40 uA at high temperature (125°C). We compare the distributions of normalized $V_{th,RTS}$-amplitude considering with the location level of the trap that $V_{th,RTS@fresh}$ in fresh devices and $V_{th,RTS@stress}$ in stressed devices under both PBTI in n-MOSFET and NBTI in p- MOSFET in Fig. 6 and Fig. 7, respectively. The result shows the generation of random trap cause RTS amplitude distribution in both stress devices being enhanced. Two of different mechanisms are in random charge effects to influence the V_{th} fluctuation. One mechanism takes place in fresh devices induced by process induced random traps (PIT) while the other occurs in stress devices induced by stress induced random traps (SIT). We can get normalized $\Delta V_{th,RTS}$ distribution of stress induce random traps between post-stress and pre-stress, using the equation (1) and (2) can result of NBTI stress has a considerably broader amplitude distribution (Mean+σ= 4.75 mV) than PBTI stress (Mean+σ= 2.85 mV). Moreover, we compare the shift of threshold voltage (ΔV_{th}) between PBTI in n-MOSFET and NBTI in p-MOSFET in Fig. 8. The NBTI one shows more generation traps than that PBTI one. In addition, NBTI in p-MOSFET has a larger of transconductance (G_m) degradation than PBTI in n-MOSFET in Fig. 9. Fig. 10 shows the cause of the generation traps mechanisms of PBTI in n-MOSFET and NBTI in p-MOSFET. Therefore, the discrepancy is partially due to the generation traps in the Si/SiO_2 interface in the p-MOSFET devices while the n-MOSFET devices have the generation traps in high-κ dielectric.

For the calculation of the equivalent random trap density and the number of the occupied oxide traps of RTS for process induced and stress induced can be extracted by the equation (5), (6) and (7) in Table 2 and Table 3 respectively. The generation of random trap density and the number of the occupied oxide traps of NBTI in p-MOSFET devices was much higher than that of PBTI in n-MOSFET devices due to a larger $\Delta V_{th,RTS}$.

4. Conclusion

In Summary, an investigation and a discussion of the impact of positive and negative bias temperature instability (P/NBTI) on the threshold voltage of the Random Telegraph Signal (RTS) in advanced gate stacks is presented. Our studies use CDF to statistically calculate the equivalent traps density and the number of the occupied oxide traps of RTS. Considering process induced random traps (PIT) and stress induced random traps (SIT) in RTS amplitude distributions, suggesting that RTS of the NBTI in p-MOSFET has a larger impact on MG/HK dielectric CMOS reliability than PBTI in n-MOSFET.

Acknowledgement

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References

[1] G. Ribes et al., IEEE Trans. Dev. and Mat. Rel., (2005) 5.
[2] Kiyoshi Takeuchi et al., VLSI (2011), 130.
[3] Seng Oon Toh et al., IEDM (2009) 767.
[4] N. Tega et al., VLSI (2009), 50.
[5] J. P. Chiu et al., IEEE Electron Device Letters 33 (2012) 176.
[6] C. Monzio Compagnoni et al., IRPS (2007) 161.
[7] Nor Hisham Hamid et al., IEEE Trans. on cir. sys. ptI. 55 (2008) 245.
[8] Sanghoon Lee et al., IEDM (2009), 763.

$V_{th,RTS}$ Amplitude [7] :

PIT: $\Delta V_{th,RTS}(\text{Mean}+\sigma)=\left(\text{Mean}(\Delta V_{th,RTS@fresh})+\sigma(\Delta V_{th,RTS@fresh})\right)\left(\frac{T_{ox}-X_{trap}}{T_{ox}}\right)$ (1)

SIT: $\Delta V_{th,RTS}(\text{Mean}+\sigma)=\left(\text{Mean}(\Delta V_{th,RTS@Stress-fresh})+\sigma(\Delta V_{th,RTS@Stress-fresh})\right)\left(\frac{T_{ox}-X_{trap}}{T_{ox}}\right)$ (2)

Trap Depth [8]:

$$\frac{d\ln\left\langle\frac{\tau_c}{\tau_e}\right\rangle}{dV_G}T_{ox}=-\frac{qX_{trap}}{kT} \quad (3)$$

$$Tox=\left(T_{ox1}+\frac{\varepsilon_{ox1}}{\varepsilon_{ox2}}T_{ox2}\right) \quad (4)$$

Number of the occupied oxide traps of RTS:

$$\Delta V_{th,RTS}(\text{Mean}+\sigma)=\frac{qN_{trap}}{C_{ox}}\left(\frac{T_{ox}-X_{trap}}{T_{ox}}\right) \quad (5)$$

$$N_{trap}=\frac{C_{ox}}{q}\Delta V_{th,RTS}(\text{Mean}+\sigma)\left(\frac{T_{ox}}{T_{ox}-X_{trap}}\right) \quad (6)$$

$$\#Trap=WL\times N_{trap} \quad (7)$$

T_{ox} is the effective oxide thickness, X_{trap} is the distance of the trap from the Si-SiO_2 interface, t_c and t_e is the average capture and emission times, q is elementary charge, K is the Boltzmann constant, T is the absolute temperature. C_{ox} is the electrical gate capacitance per area, N_{trap} is the equivalent area oxide traps density of RTS, $\#T_{trap}$ is the number of the occupied oxide traps of RTS.

Table 1 $\Delta V_{th,RTS}$ Amplitude, trap depth, the number of the occupied oxide traps equation.

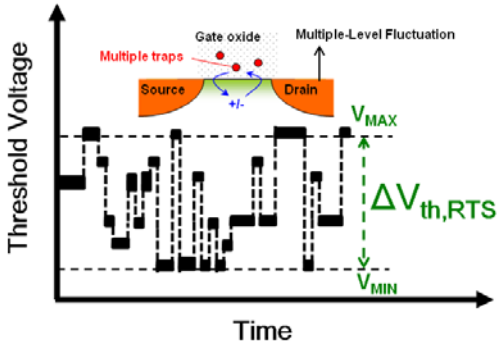

Fig. 1 Multiple-level fluctuation is corresponding to the multiple charging states of the trap in time domain.

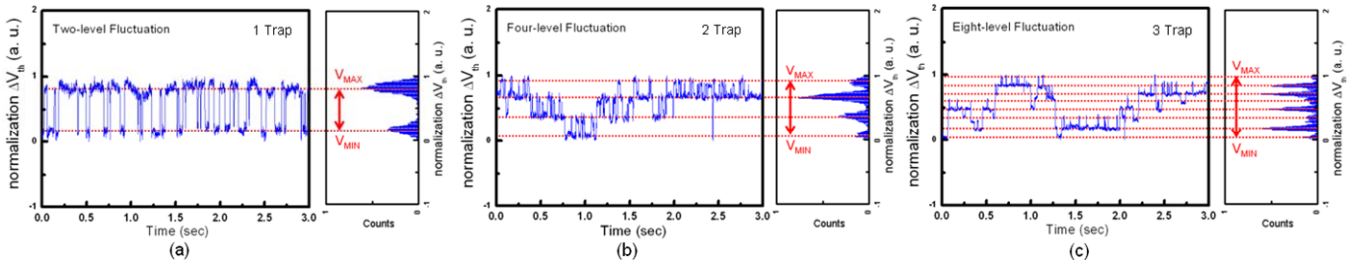

Fig. 2 (a) Two-level fluctuation, (b) Four-level fluctuation and (b) Eight-level fluctuation.

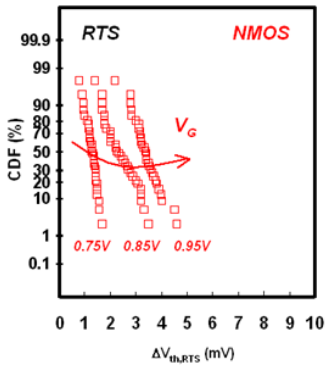

Fig. 3 CDF of charge induced $\Delta V_{th,RTS}$ for RTS in nMOSFET devices.

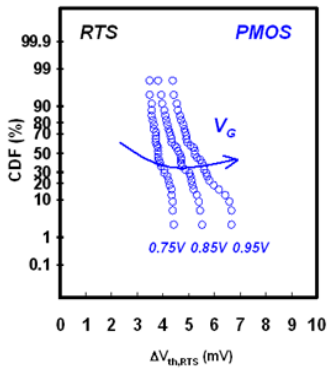

Fig. 4 CDF of charge induced $\Delta V_{th,RTS}$ for RTS in pMOSFET devices.

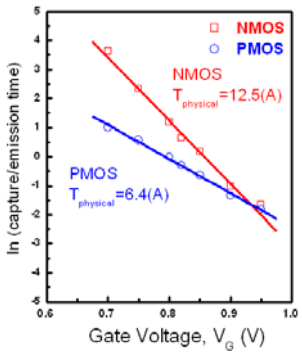

Fig. 5 Characterized depth of generated traps respect to V_G.

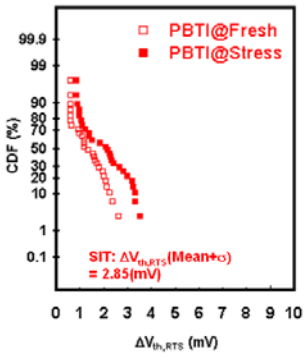

Fig. 6 CDF of$\Delta V_{th,RTS}$ in fresh devices and stress devices for n-MOSFET.

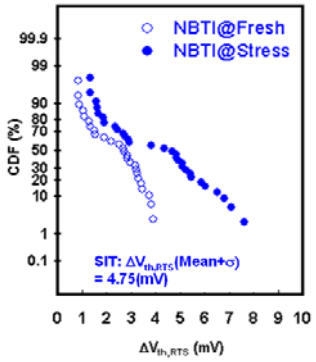

Fig. 7 CDF of$\Delta V_{th,RTS}$ in fresh devices and stress devices for p-MOSFET.

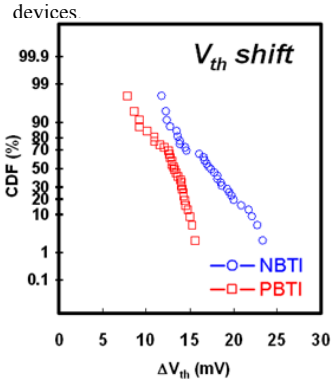

Fig. 8 CDF of V_{th} shift for PBTI in n-MOSFET and NBTI in p-MOSFET

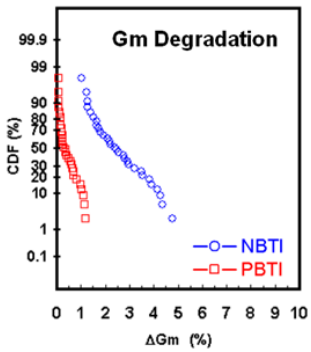

Fig. 9 CDF of G_m degradation for PBTI in n-MOSFET and NBTI in p-MOSFET.

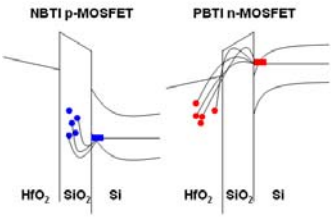

Fig. 10 Mechanisms of Charge tapping for PBTI n-MOSFET and NBTI p-MOSFET.

Process Induce Random Traps	Parameter / Device	$V_{th,RTS}$(Mean+ σ)		
		$\Delta V_{th,RTS}$(mV)	N_{trap}(#/cm^2)	#Trap(#)
	n-MOSFET	4.44	6.31E+10	4
	p-MOSFET	4.61	6.54E+10	4

Table 2 Process induced equivalent traps density and the number of the occupied oxide traps for n-MOSFETs and p-MOSFETs

Stress Induce Random Traps	Parameter / Device	$V_{th,RTS}$(Mean+ σ)		
		$\Delta V_{th,RTS}$ (mV)	N_{trap}(#/cm^2)	#Trap(#)
	PBTI n-MOSFET	2.85	4.04E+10	2
	NBTI p-MOSFET	4.75	6.74E+10	4

Table 3 Stress induced equivalent traps density and the number of the occupied oxide traps for PBTI n-MOSFETs and NBTI p-MOSFETs