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Ultralow-Voltage Operation SOTB Technology toward Energy Efficient Electronics

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Abstract

Ultralow-voltage (ULV) CMOS with high efficiency in energy can extend the opportunity of using the electronic devices such as ubiquitous sensor network. The main issues for highly efficient operation of the scaled CMOS are reducing characteristic variability and enabling adaptive control of performance and power at voltages as low as possible. To solve these issues, we are developing the silicon-on-thin-buried-oxide (SOTB) devices. This paper shows features of the SOTB, transistor technology dedicated to ULV operation, circuit design for SOTB and discusses on the performance projection and ULV application with the SOTB.

1. Introduction

Energy efficiency of CMOS circuits is an important issue of promoting both green "by" ICT as well as green ICT. It is well-known that the operating voltage (V_{dd}) is primarily important parameter for reducing the energy per operation in the CMOS circuits. As shown in Fig. 1, energy (E) is sum of active and leakage energy. With decreasing V_{dd}, the leakage energy relatively increases because the operating speed decreases. The minimum energy (E_{min}) point is roughly at around V_{dd}=0.4 V in general for the CMOS circuits. It is ideal that all the transistors in each circuit operate under the condition of E_{min}. Most of the circuits, however, do not operate under such a condition because the speed at E_{min} is generally too low. The adaptive-back-bias technique [1] is a strong way to maximize the energy efficiency because of its flexible control of speed and power.

The current scaled CMOS faces serious problems regarding V_{dd} reduction. The V_{dd} reduction trend is retarded at around 1 V. The main causes are increasing threshold voltage (V_{th}) variability and the speed/leakage trade-off. There are many variability sources, among them, the local variability caused by the random-dopant fluctuation (RDF) is a more serious problem and cannot be reduced in the conventional bulk CMOS [2]. In order to solve the above problems, we are developing a novel transistor structure, named silicon on thin buried oxide (SOTB) [3,4].

Schematic cross section of the SOTB is shown in Fig. 2. This structure is a kind of fully depleted silicon on insulator (FDSOI). Thicknesses of SOI and buried-oxide (BOX) layers are both very thin (~10 nm) to improve short-channel-effect immunity and back-gate-bias controllability. Channel impurities are implanted into the silicon substrate (well region) through the SOI and BOX layers to control V_{th} while the impurity density in the SOI layer is kept low. This impurity profile is essential for reducing the RDF variability. In addition to the substrate doping, V_{th} is also controlled by a voltage via the back-gate terminal. Another important feature is hybrid SOTB/bulk integration. Thanks to the thin SOI and BOX layers, the conventional bulk transistors can easily be fabricated only removing these layers. This feature is very important for the circuit design because the conventional circuits that uses bulk CMOS can be ported with a minimum change. Peripheral circuits, operated at higher voltages than the SOTB's maximum voltage (~1.5 V), and electrostatic-discharge protection circuits are in the bulk region.

2. Transistor technology for ULV operation

It is required to control V_{th} specifically for the ULV operation. We designed a detailed SOTB structure for the ULV operation of minimum V_{dd} at 0.4 V by using device simulation [5]. In order to control the V_{th} properly, a combination of the substrate doping and effective work function (EWF) control of the gate electrode is useful. We chose poly-silicon / high-k / SiON gate stack because it has adequate EWF (around quarter gap) for the ULV operation and its fabrication process is cost effective [6]. With this process technology, the transistor characteristics were optimized for the ULV operation as shown in Fig. 3. We fabricate triple V_{th} levels of transistors in a series of the process by changing the impurity density.

3. Demonstration of ULV operation of SRAM

We have demonstrated significant reduction of the V_{th} variability. The Pelgrom coefficient (A_{VT}) [7] (index of variability) of the SOTB is about 1.2-1.3 mVμm [8], that is less than half of the bulk. Figure 4 compares the A_{VT} values as a function of gate-oxide thickness (T_{inv}) because A_{VT} is proportional to T_{inv}. Data in the figure except for SOTB are collected from the literatures published in recent three years. Three lines denote linear regression of the bulk, FinFET, and FDSOI data. The SOTB exhibit the smallest A_{VT} values among them. The variation of on-state current is also important and is shown to be very small [9]. Moreover, we measured the V_{th} variation of one-million transistors [8] as shown in Fig. 5 and confirmed regular distribution showing the normal-distribution behavior without dropout transistors. This means a large-scale integration of SOTB is secured with our fabrication process.

Thanks to the significant reduction of the variability, as shown in Fig. 6, we successfully demonstrated 2-Mbit static random access memory (SRAM) operation at V_{dd} down to record-low 0.37 V [8]. The SRAM is most difficult circuit to operate at low voltage because it is very sensitive to the variability of transistors. The same SRAM circuit fabricated by the conventional bulk CMOS process exhibits the minimum operation voltage of around 0.8 V. The effect of the variability reduction is very clear.

4. SOTB circuit design and application

The design flow for the SOTB is basically the same as the conventional one. The standard logic cell library is important to the logic IC design. We have prepared the library suited for the SOTB characteristics and ULV operation. The ring-oscillator results (of the standard cells) showed that the SOTB exhibits higher speed and smaller delay valiability at ULV than the bulk [10]. Using our newly furnished design flow, several ULV circuits were designed. Significant power reduction was demonstrated by the post-layout timing and power analysis. As an example, the advantage of the SOTB was shown in the reconfigurable accelerator named cool mega array (CMA). The bulk CMA operates at 1.2 V and 200 MHz, and the SOTB version operates at 0.4 V and 50 MHz [11]. The power of the SOTB CMA is roughly 1/10 of the bulk CMA. The total energy considering both the operation power and the leakage power of the SOTB CMA is 40% of the bulk CMA [11].

Design from the application viewpoint is important, especially for ultralow power (ULP). The ULP design naturally prefers ULV operation to decrease E. Because of a smaller voltage margin of the ULV operation, both device specification and consideration of operating margin may become strict and strongly depend on the application requirement. We have finished the proto-type design of the ULV micro-controller chip as shown in Fig. 7. This chip can be connected with sensors and an rf module for the sensor-network node. By taking advantage of the ULP capability of our SOTB micro-controller chip, named "Perpetuum-Mobile", the sensor node is expected to operate for a long period with a single battery or further longer operation with an energy harvester.

5. Summary

Silicon on thin buried oxide (SOTB) is suitable for the ULV operation thanks to its small variability and back-gate bias controllability. We have demonstrated significant variability reduction with large-scale integration of SOTB, ULV (down to 0.4 V) operation of SRAM, and reducing power consumption of logic circuit. Many ultralow-power applications such as sensor-network node are expected to be implemented with this SOTB technology.

Acknowledgment

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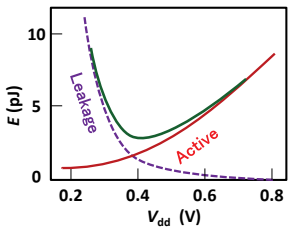

Fig. 1 Energy per operation as a function of V_{dd}.

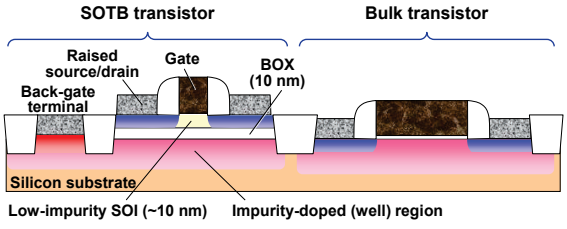

Fig. 2 Schematic cross section of SOTB and co-fabricated bulk transistors.

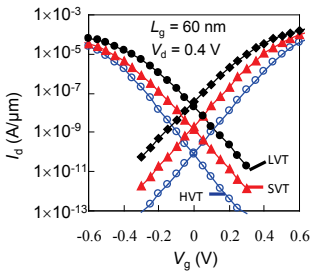

Fig. 3. I_d-V_g characteristics of N and PMOS. HVT, SVT, and LVT denote transistors of three V_{th} levels.

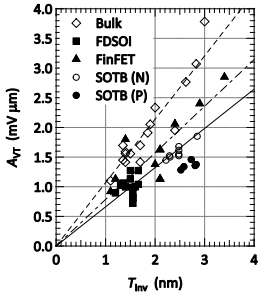

Fig. 4 Benchmark of V_{th} variability (A_{VT}).

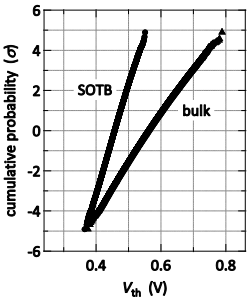

Fig. 5 V_{th} distribution of 5-M transitors.

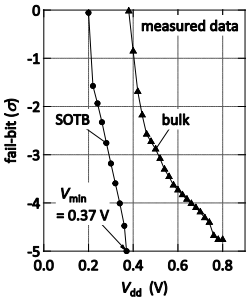

Fig. 6 Fail-bit count as a function of V_{dd}.

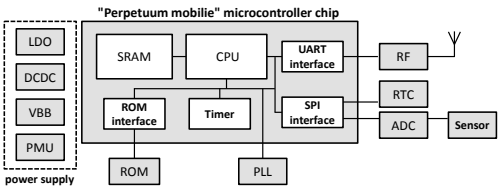

Fig. 7 Block diagram of "Perpetuum mobile" microcontroller for a sensor-node application. (RTC: real time clock, PLL: phase locked loop, ADC: analog to digital converter, LDO: low dropout regulator, DCDC: dc-dc converter, VBB: substrate-bias generator, PMU: power management unit, SPI: serial peripheral interface, UART: universal asynchronous receiver transmitter)