

Comparison of Minimum Operation Voltage (V_{min}) in Fully Depleted Silicon-on-Thin-BOX (SOTB) and Bulk SRAM Cells

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Abstract

The minimum operation voltage (V_{min}) of intrinsic channel fully depleted (FD) silicon-on-thin-BOX (SOTB) SRAM cells are measured and compared with conventional bulk SRAM cells in order to directly compare the worst cells. It is confirmed that the worst V_{min} of 1k SOTB SRAM cells is half of that of 1k bulk cells, which is a great advantage of SOTB SRAM for lower power and lower voltage operation.

1. Introduction

One of the most significant barriers for further supply voltage (V_{DD}) scaling in SRAM is the random variability of transistors [1-6]. The minimum operation voltage (V_{min}) in large scale SRAM cell array is much higher than that in logic circuits [7], which obstructs low voltage operation of SRAM and forces very complicated circuit design. One of the solutions for V_{min} reduction is the introduction of intrinsic channel FD SOI or SOTB FETs that have drastically smaller random threshold voltage (V_{TH}) and drain current variability than conventional bulk FETs [8-9]. Actually, we have recently achieved ultra-low voltage operation of 2M bit SOTB SRAM at 0.37V [10].

The stability of SRAM cells is usually characterized by static noise margin (SNM) [1-6]. However, since the stability of SRAM array is determined by the worst cell in the cell array, it is hard to quantitatively compare the cell stability by merely SNM in different technologies.

In this study, " V_{min} of the cell" is measured. V_{min} 's of 1k FD SOTB SRAM cells are intensively measured and directly compared with those in 1k bulk SRAM cells. It is found that the worst V_{min} of SOTB SRAM cells is half of that of bulk cells thanks to smaller random V_{TH} variability.

2. Measurements

SRAM device-matrix array (DMA) SRAM TEG [5-6] with intrinsic channel SOTB FETs was fabricated by the 65nm technology [10-11]. Terminals for V_{DD} , WL, two BLs, and two storage nodes (VL and VR) can be accessed (Fig. 1), so that all 6 transistors as well as SNM can be measured. The SOI thickness is 12nm, BOX thickness is 10nm, and T_{INV} is 2.8nm. For reference, conventional bulk SRAM DMA TEG with the same dimensions was also fabricated. Average V_{TH} 's of SOTB and bulk FETs are adjusted to the same value (approximately 0.29V) by substrate bias for fair comparison.

V_{min} of each cell was measured by the following method [12]. Initially, HIGH was written to one of the storage nodes (VL, for example). Then, V_{DD} was lowered and it was checked when the state of VL was flipped. During this procedure, both word line (V_{WL}) and bit line voltages (V_{BL}) were kept at V_{DD} . The same operation was done for the other node (VR). V_{min} of the cell is defined as the minimum V_{DD}

where the states in both cases are not flipped. It turned out that V_{min} 's of some of very stable cells could not be measured, because the cells were too stable ($V_{min} < \sim 0.1V$ for SOTB) and there were forward pn-junction current due to substrate bias ($V_{min} < \sim 0.3V$ for bulk).

3. Results

Fig. 2 shows V_{TH} distributions of cell transistors in 1k SOTB and bulk SRAM. Obviously, SOTB FETs have smaller V_{TH} variability. Before measuring V_{min} 's, SNMs were measured. Fig. 3 shows butterfly curves of 1k SOTB and bulk SRAM cells at $V_{DD} = 0.4V$ and Fig. 4 shows SNM distributions at $V_{DD} = 0.4V$. SOTB cells have clear "eyes" in butterfly curves even at 0.4V, while many bulk cells show zero SNM at 0.4V, which makes the direct quantitative comparison of the worst cells very difficult.

Fig. 5 shows the correlation between measured SNM and V_{min} . Good correlations are found, especially in unstable cells with high V_{min} 's. Please note that the worst V_{min} in 1k cells is 0.242V and 0.482V for SOTB and bulk, respectively. This is the direct quantitative comparison of cell array between SOTB and bulk. By utilizing SOTB, V_{min} of cell array can be reduced by half, which is a great advantage of SOTB SRAM over bulk SRAM.

Fig. 6 shows butterfly curves of a stable cell ($V_{min} = 0.138V$) and the worst cell (0.242V) of SOTB. The stable cell has a clear eye even at 0.2V, while the worst cell has no eye at 0.2V, as expected. Fig. 7 shows butterfly curves of the worst bulk cell, which shows no eye even at 0.4V.

4. Conclusions

The stability of the worst cells in SOTB and bulk SRAM is directly compared by measuring V_{min} 's of the SRAM cells. It is found that the worst V_{min} can be reduced by half by introducing SOTB thanks to reduced V_{TH} variability.

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