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The Demonstration of Complementary Tunnel FET with Vertical Tunneling Junction Structure Compatible with Si CMOS Platform

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Abstract

In this paper, we have demonstrated vertical tunneling junction FETs (V-TFETs) with conventional all-Si CMOS compatible process for the first time. By utilizing counter-doped surface pocket (SP) in source extension (Ext.) region, vertical tunneling junction was successfully formed under the gate overlap region only by common ion implantation technique. It achieved well-balanced complementary TFET (CTFET) with improved tunneling device characteristics (I_{ON}/I_{OFF}, *S.S.*, V_{TH}). The guideline of SP and Ext. design was also presented to avoid undesirable thermal diffusion transport. The realization of shallow and abrupt P-N junctions by introducing carbon co-doping, FLA and extension last integration scheme improved performances further and demonstrated record high I_{ON}/I_{OFF} ratio (> 10^6) among all-Si TFETs in n-type V-TFET.

Introduction

Tunneling field effect transistors (TFETs) have attracted much attention for ultra-low power applications thanks to its possibility of overcoming the limitation of subthreshold swing (*S.S.*) in MOSFET less than 60 mV/decade. Previous reports in P-i-N lateral TFET (L-TFET), however, have suffered from low I_{ON}/I_{OFF} ratio and unsatisfactory *S.S.* especially in n-type FETs [1]. Unbalanced characteristics of the n-, and p-type L-TFET impede the realization of complementary TFET (CTFET) which is essential feature for practical usage. To improve TFET performances, enhancement of gate controllability by utilizing vertical tunneling parallel to the gate field has been proposed [2-7]. Although some vertical tunneling mode TFETs (V-TFETs) have been reported, those tunnel junctions were formed by distinctive processes such as dopant segregation [5], non-self-aligned gate formation [6,7] and extremely thin film formation with epitaxial process [7]. In this paper, we demonstrate V-TFET fabricated with all-Si CMOS compatible process, i.e., vertical tunneling P-N junction was formed only by ion implantation (I/I). The significant improvement of tunnel operation have been confirmed both on n- and p-type V-TFETs. The highest I_{ON}/I_{OFF} ratio was achieved in optimized n-type V-TFET reported to date.

Device Fabrication

Both n/p-type L-TFETs and V-TFETs were fabricated on p-type SOI (t_{si} = 85 nm) substrates with Si CMOS compatible process (**Fig. 1**). Following the formation of Poly/SiON gate stack (EOT = 2 nm), lateral or vertical tunneling junction was formed in source regions for each TFET. For V-TFET, counter-doped surface pocket (SP) was formed in extension (Ext.) regions to make vertical P-N junction under the gate. As and BF_2 were implanted into SP regions for n- and p-type V-TFETs, respectively. In order to obtain sufficient gate overlap on vertical tunneling junction, offset spacer was not utilized for V-TFETs. After the formation of gate sidewall spacer, contact junctions were formed in source and drain regions compensating SP regions outside of the gate electrode. To evaluate practical TFET performance, the typical gate length of 120 nm is focused here (**Fig. 2 (a)**).

Results and Discussions

(1) Optimization of V-TFET: Improved ON-current (I_{ON}) and reduced *S.S.* were achieved in V-TFETs compared with L-TFETs (**Fig. 3**). Well-controlled threshold voltage (V_{TH}) was also confirmed in V-TFET. These results indicate that appropriate vertical P-N junctions have been successfully formed under the gate. This is also confirmed by process simulation analysis (**Fig. 2 (b)**). Remarkably, the improvement is prominent in n-type TFETs, and well-balanced CTFETs were achieved in V-TFET structure.

The formation of SP is the key for the device optimization in V-TFETs. As SP dosage increases, I_{ON} tends to become higher (**Fig. 4**). However, I_D–V_G characteristics in V-TFETs with higher SP dosage show constant *S.S.* behavior (**Fig. 5**) and significant temperature dependency (**Fig. 6**). Theoretically, *S.S.* in MOSFETs is determined by $\ln 10 kT/q \times (1+C_{dm}/C_{ox}) > 0.20$ (mV/dec.) × *T*. Here, temperature coefficient of 0.24 (mV/dec.·K) was confirmed in V-TFET (inset in **Fig. 6**), This indicates that MOSFET carrier transport could be involved in V-TFET if SP doing is high. This is explained by band diagrams shown in **figure 7**. Unintentional potential barrier is created in PN-PN junction under the gate in the strong SP case (**Fig. 7 (a)**). This enhances the component of thermal diffusion transport and makes it impossible to overcome *S.S.* limit of MOSFET. On the other hand, in the weak SP case (**Fig. 7 (b)**), SP region can be fully depleted so that the potential peak disappears [8]. In order to fully utilize the advantage of TFET, vertical P-N tunneling mode should be dominant in subthreshold region. To clarify the FET operation mode, temperature dependence of *S.S.* on various SP and Ext. dosages was widely investigated. As shown in **Fig. 8 (a)**, three operation modes have been experimentally categorized with respect to magnitude of slopes in *S.S.* vs. temperature (as shown in **Fig. 8 (b)**). As expected, excessive SP dosages against Ext. dosages leads to MOSFET mode operation (Region A). In contrast, insufficient SP dosages could not form vertical P-N junction and approaches L-TFET mode (Region C). It is important to optimize SP and Ext. conditions within the guidelines of desirable V-TFET operation.

(2) Further improvements: In order to improve the performance within V-TFET operation window, one of the promising approaches is to form shallow SP [2, 9]. However, it is difficult to control SP thickness only by SP I/I condition due to interdiffusion between SP and Ext.. Carbon co-implantation was adopted for SP and Ext. formation to suppress boron diffusion and makes SP design window wider. Improved $I_D - V_G$ characteristics were confirmed both in n- and p-type V-TFETs with carbon co-implantation (**Fig. 9**), indicating better *S.S.* and incredibly increased I_{ON} with keeping symmetric n/p operations. I_{ON}/I_{OFF} ratio of more than five decades was achieved in n-type V-TFET which is one of the best performances in Si TFETs (**Table. 1**). SIMS analysis indicates that C-doping modulates dopant profiles and creates shallower SP less than 10 nm (**Fig. 10**).

In order to boost V-TFET performance further, extension-last (EL) integration scheme with flash lamp annealing (FLA) was adopted to obtain abrupt tunnel junction. In this scheme, SP and Ext. (with Carbon) were formed after contact junction formation to minimize the thermal budget for tunnel junction formation. EL-V-TFET with FLA enables dramatic improvement in I_{ON} (**Fig. 12**). Here, the *S.S.* improvement was minimal due to the insufficient defect recovery during FLA process. So, further optimization of process condition is required; however, EL-V-TFET with FLA still achieved I_{ON}/I_{OFF} ratio of >10^6, which is the record number among reported data in all-Si TFETs (**Table. 1**).

Conclusion

We have demonstrated vertical tunneling junction FETs (V-TFETs) with all-Si CMOS compatible process for the first time. Precisely controlled vertical P-N junctions by ion implantation dramatically improved performance both on n- and p-type V-TFETs, and enabled the formation of well-balanced CTFET. With additional thermal budget control, record high I_{ON}/I_{OFF} ratio (> 10^6) among all-Si TFETs has been achieved in n-type V-TFET.

Acknowledgments

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References

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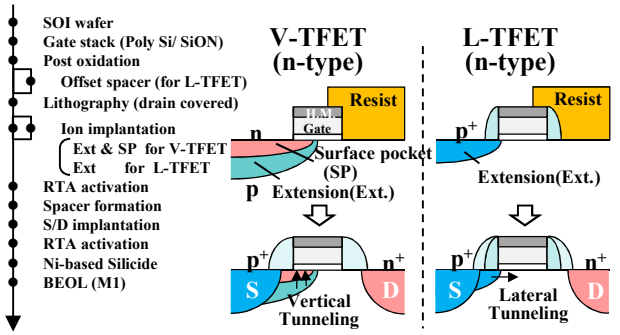


Fig.1. Process flow and schematic device structures of n-type V-TFET and L-TFET. For V-TFET, counter-doped surface pocket (SP) was formed above extension (Ext.) region by ion implantation (I/I). The SP is compensated by source contact junction I/I and isolated from contact. P-type V- and L-TFETs were also fabricated with opposite type of dopants.

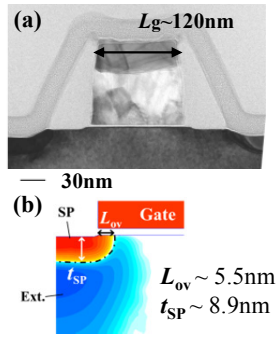


Fig.2. (a) x-TEM image of V-TFET. The typical gate length of 120 nm was evaluated in this report. **(b)** Simulated SP and Ext. regions in a certain I/I condition.

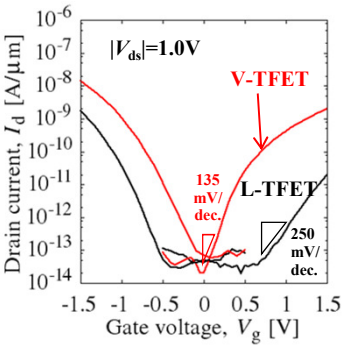


Fig. 3. Typical I_d-V_g characteristics of n- and p-type TFETs. Especially for n-type, improved ON-current (I_{ON}) and reduced *S.S.* were achieved in V-TFETs compared with L-TFETs. In p-type V-TFETs, *S.S.* increase from 155 to 178 (mV/dec.).

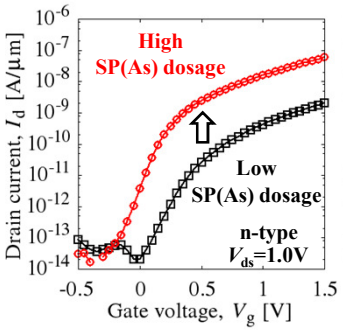


Fig. 4. I_d-V_g characteristics in n-type V-TFETs with high and low SP dosages. Increased ON-current (I_{ON}) and steeper *S.S.* are observed in high (1×10^{15} atoms/cm^2) SP dosed V-TFET.

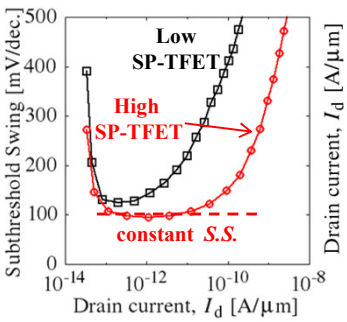


Fig. 5. *S.S.* vs. I_d plots of the curves in **Fig.** 4. The V-TFET with high-dosed SP shows constant *S.S.* over three orders of current changes, like in sub-threshold region of MOSFETs

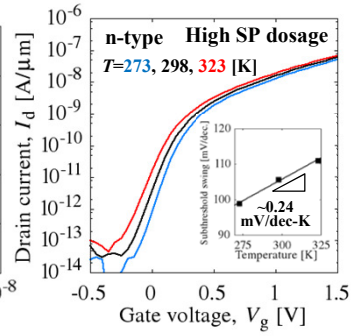


Fig. 6. I_d-V_g characteristics in n-type V-TFETs with high SP dosage and its temperature dependence of *S.S.* (inset). This *S.S.*-Temp. slope reveals similar behavior in MOSFETs.

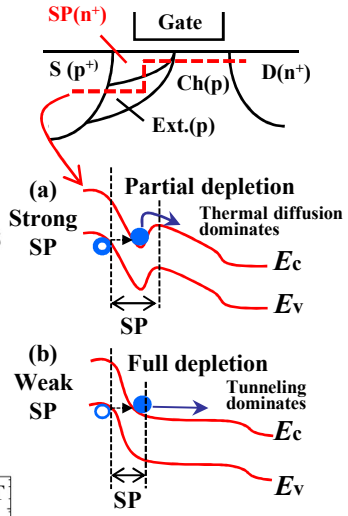
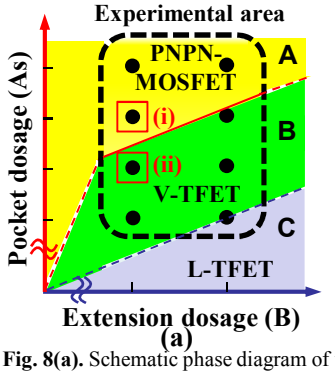


Fig. 7. Energy band diagrams along the carrier flow shown in device structure (dashed line). **(a)** Strong SP condition, **(b)** Weak SP condition. The mode of the carrier transport is affected by its potential shape based on SP thickness and concentration.



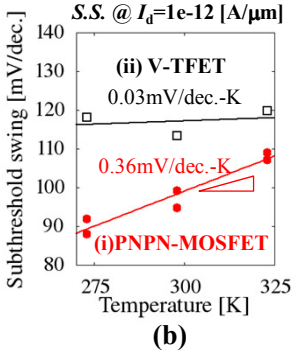


Fig. 8(a). Schematic phase diagram of three operation modes categorized with respect to magnitude of the slopes in *S.S.* vs. temperature. In region A, the value of the *S.S.* vs. temperature slope are greater than the value 0.20 of the MOSFET theoretical limit. **(b)** *S.S.* vs. temperature of the devices whose I/I conditions correspond to the points shown in Fig. 8(a).

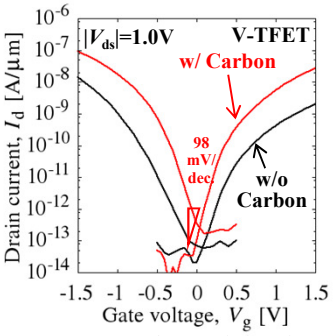


Fig. 9. I_d-V_g characteristics of V-TFETs. With carbon co-I/I, *S.S.* of the n- and p-TFETs are improved to 98 and 121 (mV/dec), respectively and prominent I_{ON}/I_{OFF} ratio of 5×10^5 in n-type V-TFET was achieved. It was confirmed the slopes of the *S.S.* vs. temperature were less than 0.20 (not shown).

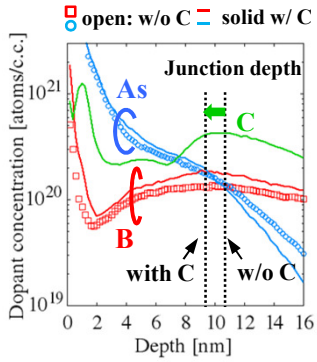


Fig. 10. SIMS profiles with (line) and without (open symbol) C co-implantation. With C, thinner SP of less than 10 nm was formed.

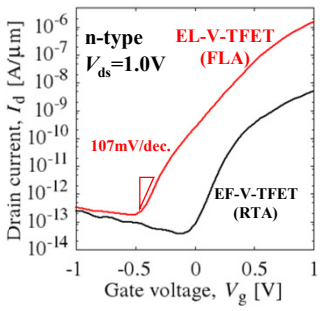


Fig. 11. Reduced thermal budget EL-V-TFET with FLA enables dramatic improvement in I_{ON}.

nTFET	[7]	[9]	[10]	This work	
Structure	Vertical Epi-ch	(Lateral) JTFET	Hetero source	EF-V-TFET w C co-II	EL-V-TFET w FLA
Material	Si	Si	SOI w Ge	SOI	SOI
EOT (nm)	1.3	5	3	2	2
V_d (V)	1.0	0.6	0.5	1.0	1.0
**I_{ON}(μA/μm)	0.008	0.04	2.5	0.02	1.2
*I_{OFF}(μA/μm)	1.0E-07	1.0E-07	1.0E-07	4.0E-08	2.0E-07
I_{ON}/I_{OFF}	8.0E+04	4.0E+05	2.5E+07	5.0E+05	6.0E+06
S.S. (minimum)	72	36	~40	98	107

*I_{OFF}: minimum I_d (V_g at I_{OFF} is defined as V_{off})
**I_{ON}: I_d at V_g=V_{off}+1.5V

Table I. Performance comparison in n-type TFETs between this work and published results. EL-V-TFET with FLA achieved the highest I_{ON}/I_{OFF} ratio among all Si TFETs.