CMOS-Compatible Mesa-Etched Ultrathin Epitaxial Channel Tunnel Field-Effect Transistors

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Abstract
CMOS-compatible mesa-etched ultrathin epitaxial channel architecture for tunnel FET is proposed. The performance enhancement in the novel architecture by a synthetic field effect is experimentally revealed by fabricating Si p and n TFETs.

1. Introduction
A tunnel field effect transistor (tunnel FET, TFET) is one of the promising candidates for steep subthreshold swing (SS) devices. [1] In TFET fabrication, it is essential to prepare an abrupt dopant profile in a source tunnel junction. To realize such abrupt dopant profile, epitaxial growth is most effective technique. [2-6]

In the epitaxial growth technique, dopant modulated layers are to be stacked to vertical growth direction against the wafer. As a result, direction of tunneling, which is across the source/epitaxial channel interface, should be “vertical”. [Fig. 1(b)-(c)] To integrate epitaxial channel interface to CMOS devices, modified architectures different from conventional “lateral” TFETs are indispensable.

In our previous study, we have fabricated the epitaxial channel TFETs with parallel tunneling against gate electric field. [Fig. 1(c)] For more performance enhancement, in the present study, we propose novel mesa-etched ultrathin epitaxial channel TFET architecture. [Fig. 1(d)] We evaluated the effectiveness of this novel architecture by experimentally fabricating Si p- and n-TFETs. In addition, we revealed the performance enhancement of the TFETs by the synthetic electric field (SE) effect at the edges of the mesa-etched channel. [7]

2. Experimental
As shown in Fig. 1(d), an epitaxially grown double layer body is used as a framework. The process flow is based on a source/drain-first FET process. (Fig. 2) The source and drain are preferentially created by ion implantations (I/I). An undoped thin Si channel is epitaxially grown on source/drain-first SOI wafers. The stacked epitaxial channel interface is outcropped at the sidewall by body mesa-etching as three-dimensional channel. After cleaning, high-k gate insulator and gate electrode are deposited covering three-dimensional channel, forming a tri-gate electrode configuration.

In the tri-gate configuration, both of top and side gate electric fields can be cooperative. [Fig. 1(d)] At the top gate, the epitaxial channel layer acts as a parallel-plate tunnel capacitor, initiating band-to-band tunneling (BTBT) parallel to the gate electric field. At the side gates, the BTBT can be initiated across outcropped source/epitaxial channel interface, which is perpendicular to the side gate electric field. In addition, the electric field from top gate is also applied to the tunnel junction, and totally synthesized electric field strength initiates enhanced BTBT. (See next section) [7]

3. Results and discussion
Cross sectional transmission electron microscopy (X-TEM) image (Fig. 3) of the channel cross-section revealed that an ultrathin epitaxial channel could be directly grown on highly doped source surface. In magnified image, a small number of defects can be visible at the interface. The image of the gate cross-section reveled that the source well overlapped the gate electrode intermediate by the ultrathin epitaxial channel and gate insulator layers. Distributions of electric fields in the channel were calculated by simulation [8]. It shows that electric field is stronger at the edge regions, which can be explained by the SE effect. (Fig. 4). When the channel is thick (D_{CH}=50 nm) and wide (W_{CH}=50 nm), the maximum electric field is small and is caused only by the perpendicular electric field. Thinning the channel thickness (D_{CH}=10 nm) increases the parallel electric field, and the maximum electric field is enhanced. This effect is further enhanced when the channel width is scaled from 50 nm to 20 nm.

Fig. 5 shows I_{D}-V_{G} characteristics of the TFETs with and without the SE effect. The SE-TFET exhibits 10-100 times larger I_{D} than those of parallel electric field TFETs. [4-6] Fig. 6(a) shows relation between I_{D} and W_{CH} in SE-TFETs. By reducing epitaxial channel thickness, I_{D} component at channel edge region (intersection to the y-axis) increased. This clearly reveals performance enhancement by SE effect. Fig. 6(b) shows relation between I_{D} per channel width and channel thickness in the SE-TFETs, which clearly reveals that the performance is better when the channel is thin and narrow. Fig. 7 shows I_{D}-V_{G} characteristics of the p- and n-SE-TFETs with thin channel thickness and width. By scaling both epitaxial channel thickness and channel width, increased drain currents are obtained in the SE-TFETs. However, the performance of the n-TFET is worse than that of p-TFET, which should be the next challenging issue for CMOS operation.

4. Summary
We proposed novel mesa-etched ultrathin epitaxial channel TFET architecture for CMOS devices. At the mesa-etched side gate, the synthetic electric field effect to enhance TFET performance is revealed. Since this SE effect is localized at a narrow edge region, use of a FinFET-like device structure is promising.

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References:
Gate BOX n+ S
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TFET without SE effect
TFET with SE effect
Electric field (V/cm)
Gate electrode
Electric field enhancement
(a)

Fig. 1: Schematics of tunnel FETs fabricated by (a) ion implantation (I/I) and (b) & (c) epitaxial growth techniques. In conventional TFET fabricated by I/I, tunnel direction is "lateral" which is perpendicular to the gate electric field. In recessed epitaxial channel TFET, relation between tunnel direction and gate electric field is similar to that of (a) but tunnel direction is "vertical" against wafer. In epitaxial channel TFET fabricated on preferentially ion-implanted wafer, the tunnel direction is vertical which is parallel to the gate electric field. In novel mesa-etched epitaxial channel TFET shown in (d), the tunnel direction is parallel to the top gate field and perpendicular to the side gate field.

Fig. 2 Schematic process flow of the novel mesa-etched ultrathin epitaxial channel with the S/D first and junction-last processes. Note that the process temperature after the epitaxial growth of Si channel is less than 700 °C.

Fig. 3 Typical X-TEM images of the mesa-etched ultrathin epitaxial channel TFET. (a) Channel cross-section, (b) Magnified epitaxial channel interface, and (c) Gate cross-section.

Fig. 4 Simulation of electric field in the mesa-etched ultrathin epitaxial channel (see Fig. 1(d)). (a) Cross-sectional distribution of electric field in a channel with \( W_{ch} = 20 \text{ nm} \) and \( D_{min} = 10 \text{ nm} \). (b) Impact of top and side gate electric fields for the synthetic electric field. (c) Impacts of channel dimensions on the electric fields. In case of a thick channel, the top gate electric field is small and only the side gate electric field at the edge region is large. With the thinning of epitaxial channel thickness, the electric field increases totally. Increase of electric field at edge region is the synthetic electric field effect. This effect is further enhanced by the scaling of channel width.

Fig. 5 Comparison of \( I_{off-V_{ch}} \) characteristics (\( V_{G} = -1 \text{ V} \)) of the parallel electric field TFET (circles) and the SE-TFET (diamonds). \( I_{off} \) and \( W_{ch} \) are 1000 and 150 nm, respectively. The insets show schematics of the gate electrode configurations.

Fig. 6 (a) Relationships between \( I_{o} \) and \( W_{ch} \) of the p-SE-TFETs. \( D_{min} \) are 10 nm and 16 nm. The intersections at the y-axis represent the drain currents at the edge regions in the mesa-etched ultrathin epitaxial channel. (b) Relationship between \( I_{o} \) per channel width and \( W_{ch} \) in the p-SE-TFETs. A FinFET-like thin \( W_{ch} \) structure is promising for the enhancement of \( I_{o} \).

Fig. 7 \( I_{off-V_{ch}} \) characteristics of p- and n-SE-TFETs. \( I_{off} \) and \( W_{ch} \) are 100 and 60 nm, respectively.