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$In_{0.53}Ga_{0.47}As$ Diodes for Band-to-Band Tunneling Calibration and n- and p-LineTFET performance prediction

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Abstract

Promising predictions are made for III-V TFET, but there is still a large gap between simulation and experiment [1]. Calibration efforts are ongoing [2,3], but the electric field at the tunnel junction is not always well known. In this paper, the band-to-band tunneling model for $In_{0.53}Ga_{0.47}As$ was calibrated with simple p-i-n diodes which have a uniform electric field in the i-region. Good agreement was obtained between simulations and experimental results. The calibrated models were applied to predict $In_{0.53}Ga_{0.47}As$ n- and p-lineTFET performance.

1. Introduction

The TFET is a promising candidate to replace the MOSFET for future low power logic nodes. Especially III-V materials are of great interest, since they feature much higher band-to-band tunneling (BTBT) currents than their group IV counterparts due to the direct band gap and smaller effective tunnel mass [1]. The performance of different TFET configurations and materials can be predicted with semi-classical or quantum-mechanical simulations, but an accurate calibration of the models used is still missing.

2. Fabrication and characterization

A new process flow was developed for small-junction-area diode fabrication [3-5], featuring metal-free wet etching of the mesa and self-aligned p- and n-type contact deposition. $In_{0.53}Ga_{0.47}As$ p-i-n stacks were grown by MBE on 2 inch InP(001) substrates (p-doped at $5\times10^{17}cm^{-3}$) from AXT [6]. Stacks with different intrinsic thicknesses T_i were grown (9nm, 18nm, 46nm), and the p- and n-region doping levels were $2\times10^{19}cm^{-3}$ and $1.5\times10^{19}cm^{-3}$, resp. After patterning a SiO_2 hard mask (fig. 1a), the diodes were wet etched using a diluted citric acid-peroxide solution. A metal contact was then deposited self-aligned on the p-$In_{0.53}Ga_{0.47}As$, followed by Benzocyclobutene (BCB) spinning and curing (fig. 1b). The BCB was recessed and the exposed metal and SiO_2 hard mask were removed. A metal contact was then deposited on n-$In_{0.53}Ga_{0.47}As$ and patterned. Finally the exposed BCB was removed by dry etching to allow connecting to the metal contact of the p-$In_{0.53}Ga_{0.47}As$ layer (fig. 1c).

The n-type doping level $1.5\times10^{19}cm^{-3}$ was confirmed with Hall measurements. The T_i = 18nm was verified with C-V measurements (fig. 2). Dominating BTBT current in reverse bias and small forward bias was validated by weak temperature dependence, supported by negative differential resistance in forward bias at room temperature (fig. 3). The BTBT current scaled with area (fig. 4), making calibration possible. Diodes with T_i = 46nm show SRH current at onset allowing generation lifetime extraction (fig. 5).

3. BTBT calibration and TFET prediction

P-i-n diodes with abrupt doping profiles were simulated (fig. 6) [7]. The models include light hole, heavy hole and split-off bands, direct and indirect (L,X) conduction band valleys with non-parabolicity [7-9], Jain-Roulston doping dependent band gap narrowing (BGN) [10-11] and dynamic nonlocal path BTBT with direct gap parameters $A=1.57\times10^{20}$ cm^{-3} and $B=5.5\times10^{6}$ V cm^{-1} [12]. A good match was obtained between experiments and simulations (fig. 7).

Pocketed lineTFETs were simulated with these calibrated BTBT models (fig. 8) [7]. BGN was not included and therefore the predicted current is an underestimation. The n-TFET has a sub-60mV/dec swing with I_{60}=0.2μA/μm (fig. 8a) [13], while the p-TFET has a super-60mV/dec onset due to the low electron density-of-states mass of $In_{0.53}Ga_{0.47}As$ (fig. 8b) [14]. The pocketed $In_{0.53}Ga_{0.47}As$ n-lineTFET looks promising with I_{on}=290μA/μm in a supply voltage window V_{dd} of 0.5V.

4. Conclusion

$In_{0.53}Ga_{0.47}As$ p-i-n tunnel diodes with three different intrinsic region thicknesses were fabricated. The tunnel current was measured and compared to semi-classical simulations using SentaurusDevice. Good agreement was obtained from E=0.21MV/cm to 1.2MV/cm, validating the BTBT model. Predictions based on the calibrated BTBT model for the pocketed $In_{0.53}Ga_{0.47}As$ n-lineTFET showed a promising I_{on}=290μA/μm for V_{dd}=0.5V, with I_{60}=0.2μA/μm.

Acknowledgements

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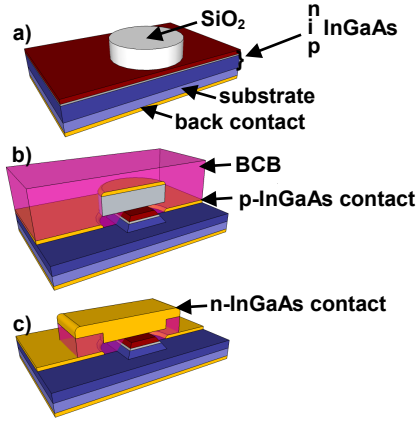

Fig 1: Fabrication of the p-i-n diodes.

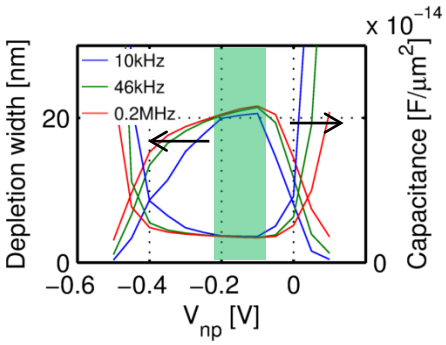

Fig 2: C-V characteristics on diodes with T_i = 18nm. In the low-current and frequency-independent C region (shaded green), the depletion width is ~20nm.

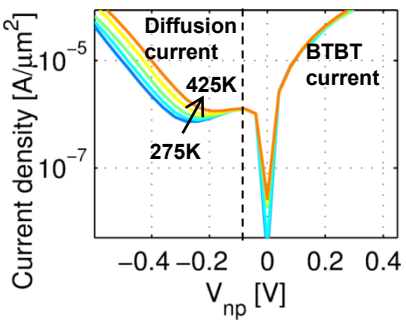

Fig 3: Temperature dependence of diode current (3.5µm^2 diode, T_i = 9nm) identifies BTBT and diffusion regimes.

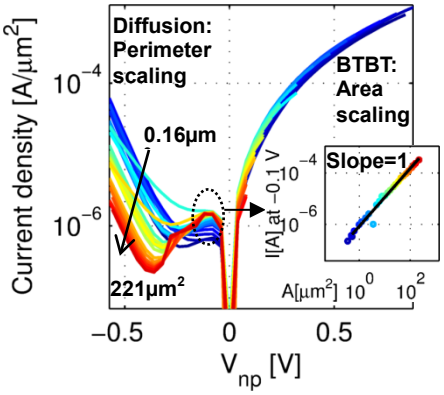

Fig 4: Areal current density in diodes of different size. Inset: I@V_{np}=-0.1V. BTBT current scales with diode area, diffusion current with diode perimeter.

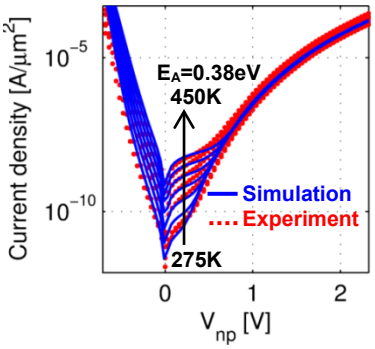

Fig 5: Temperature dependence of diode current (2.7µm^2 diode, T_i = 46nm) identifies SRH current at low reverse bias (activation energy E_A = 0.38eV, half $In_{0.53}Ga_{0.47}As$ band gap). SRH calibration yields τ_{SRH}=2.5e-14s.

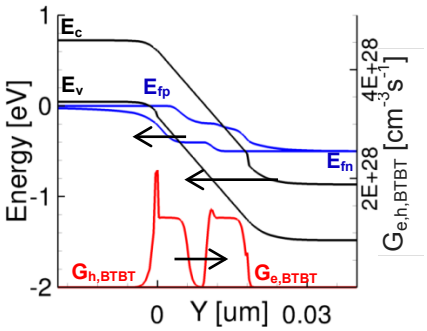

Fig 6: Band structure at V_{np}=0.5V [7], showing BTBT generation ($G_{e,h,BTBT}$) only in the uniform electric field region.

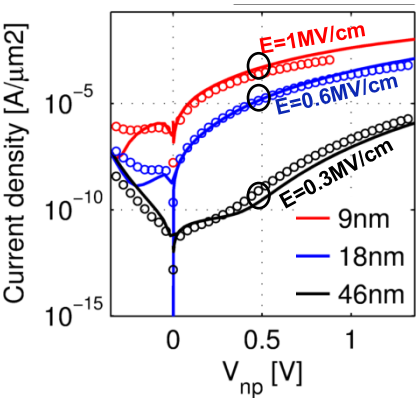

Fig 7: BTBT simulations (full lines) [7] and experimental BTBT current (circles) show a good match. The simulated electric field in the intrinsic region at V_{np}=0.5V is indicated.

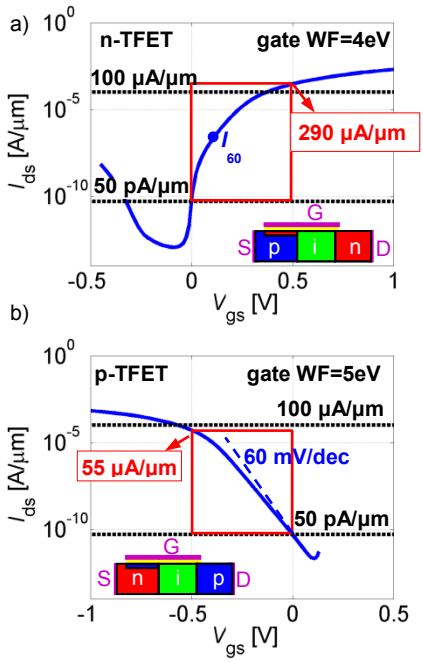

Fig 8: Pocketed a) n- and b) p-lineTFET predictions, with a) I_{60}=0.2µA/µm and b) SS~70mV/dec (EOT=0.6nm, L_{gs}=30nm, L_{chan}=50nm, t_{pock}=(a)3.4nm-(b)4.8nm, N_S=N_{pock}=(a)2x10^{20}cm^{-3}-(b)5x10^{19}cm^{-3}, V_{ds}=0.5V). The semi-classical curves were shifted according to field-induced quantum confinement [15].