

Germanium quantum-dot single-electron Coulomb blockade thermometry

Inn-Hao Chen, Ching-Chi Wang, Kuan-Hung Chen, and Pei-Wen Li

Department of Electrical Engineering, National Central University, ChungLi, Taiwan, ROC, 32001

Phone: +886-3-422-7151 E-mail: pwli@ee.ncu.edu.tw

Abstract

We realized Ge-QD single-hole transistors (SHTs) with a 10 nm QD weakly coupled to p⁺-poly-Si electrodes through a 12-nm-thick tunnel barrier of SiO₂/Si₃N₄ in a self-organized scheme. Gate and drain voltage modulations onto the Ge-QD SHT produce clear current oscillatory and plateau characteristics at temperature of 77–140 K as a result of strong Coulomb blockade effects. The well-sealed Coulomb diamond behaviors reveal distinctive tunneling spectroscopy of energy levels, strong Coulomb charge interactions, and superior Coulomb stability within the Ge QD. The remarkable normalized differential conductance dips in the G_D - V_{DS} traces at $T = 77$ –140 K appear to have a linear dependence on the electron temperature, offering a great opportunity as a primary thermometer of unprecedented sensitivity.

1. Introduction

Quantum confinement effects induce size-tunable absorption and emission frequencies, high quantum yield and photostability have made quantum dots (QDs) an active field of research and development for logics, memory, lighting, imaging, labeling and sensing. In addition to wide-accepted optoelectronics, biology and medicine stand out as the most appealing areas since bioconjugation of QDs can make them target selective. In particular, semiconductor QDs have been proposed for small-scale thermometry thanks to their strong temperature dependent photoluminescence that is able to sense temperature variations and report temperature changes remotely through optical readout. In fact, the unprecedented charge sensitivity of QD single-electron transistor (SET) offers another effective approach for the temperature detection. To further improve the sensitivity and stability of the thermometry, Coulomb blockade thermometry is proposed [1-2] based on the feature of the electric conductance characteristics of tunnel junction arrays being highly dependent on QD temperature. In particular, when $k_B T \gg \varepsilon_C$, the dynamic conductance of a junction array can be expressed as $G/G_T = 1 - (\varepsilon_C/k_B T)g(eV/Nk_B T)$, where G_T is the asymptotic conductance at high bias voltage and N is the number of junctions in series. The width of the conductance dip in the Coulomb blockade regime scales with T and N , whereas the height is inversely proportional to T .

In this paper, we report a successful demonstration of high-performance Ge-QD single-hole transistors (SHTs) that possesses satisfactory control over the charge number and transport [3]. Attendant to the high charge sensitivity also includes the ability to measure the actual electronic temperature difference across a Ge QD and to be utilized as a primary thermometer with high sensitivity.

2. Experimental and results

The Ge-QD SHT, consisting a 10 nm Ge QD weakly coupled to p⁺-poly-Si electrodes through a 13-nm-thick tunnel barrier of Si₃N₄ (EOT = 6.5 nm), is realized in a self-organized approach that has been described in details elsewhere [3]. Schematics of the designed device structure and key fabrication process flow are described in Fig. 1(a)-(b). Figure 1(c) and (d) illustrate that there is a 10nm, single-crystalline Ge QD residing between p⁺ poly-Si

source/drain electrodes via a 13-nm-thick tunnel barrier of Si₃N₄. Additionally the Ge QD also simultaneously self-aligns with gate electrode through a 43 nm-thick gate oxide. These transmission electron microscopy (TEM) micrographs clearly manifest the proposed QD self-assembly technique is able to precisely place a single QD that self-aligns with electrodes via tailored tunnel junction for practical applications.

Charge tunneling through discrete energy levels of the Ge QD appears to be well governed by gate (V_G) and drain voltages (V_{DS}) onto the studied SHT. Drain modulation produces distinctive current I_D plateaus and differential conductance G_D peaks when V_{DS} exceeds a threshold value of 0.25 V at gate bias of 0.6 V (Fig. 2(a)), and the zero-conductance gap is effectively reduced with a decrease in V_G from +0.6 to -0.6V. The tunneling current spectroscopy of the Ge QD in few-hole regime is further clarified by the Coulomb oscillatory current with respect to gate voltage at various V_{DS} . When V_{DS} is small and within the zero conductance gap (< 0.25 V), there appear three oscillatory I_D peaks within the experimental gate voltage regime (Fig. 2(b)). The first peak at $V_G = -0.66$ V refers to carriers tunneling through the ground state (E_1), the second peak at $V_G = -1.14$ V arises from hole overcoming the charging energy of $E_1 + U_1$, and the third peak at -1.85 V is produced by charging passing through the first excited state (E_2). The well-resolved Coulomb diamonds in the I_D contour plot and the distinctive undulations in the three-dimensional I_D - V_{DS} - V_G characteristics reveal strong Coulomb charge interactions and superior good Coulomb stability with the Ge QD as a result of Coulomb blockade. The estimated single-hole addition energy for the ground state from the slope ratios of the Coulomb stability diagram is 29.8 meV.

Figure 4 shows the typical measured differential conductance versus bias voltage of the Ge-QD SHT at $T = 77$ –140 K. Interestingly a sharp quantum conductance dip is observed in the G_D/G_{D0} - V_{DS} trace. The dependence of the width and depth of the conductance dip, G/G_T , on the capacitance of the Coulomb blockade junctions allows one to set the mean temperature of the QD. The full width at half maximum (FWHM) of the nonlinear conductance trace could be well-fitted by $e\delta V \sim N \times 5.44 k_B T$ [4], where N is the number of QDs in series between electrodes. The fitted value of $N \sim 0.9$ is very close to unity and the height of conductance dip is inversely proportional to T , indicating a good temperature linearity for the Ge-QD SHT that could be used as a sensitive bolometer sensing the local temperature of the Ge QD for nano-scale thermometry.

Acknowledgements

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References

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- Pad layers deposition (poly-Si/Si₃N₄/SiO₂)
- Active area definition
- Nano-gap definition (~300 nm)
- Nano-electrode definition (~100 nm)
- SiO₂/Si₃N₄ spacer formation
- Poly-SiGe deposition & etching back
- Poly-Si etching back
- Ge nano-rod definition (~50 nm)
- Ge QD formation
- Poly-Si gate definition
- Metallization

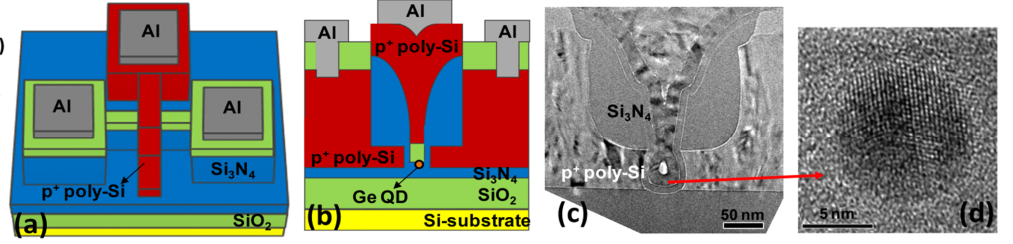


Fig.1 (a)/(b) schematic device structure and (c)/(d) cross-sectional TEM images of fabricated Ge-QD SHTs.

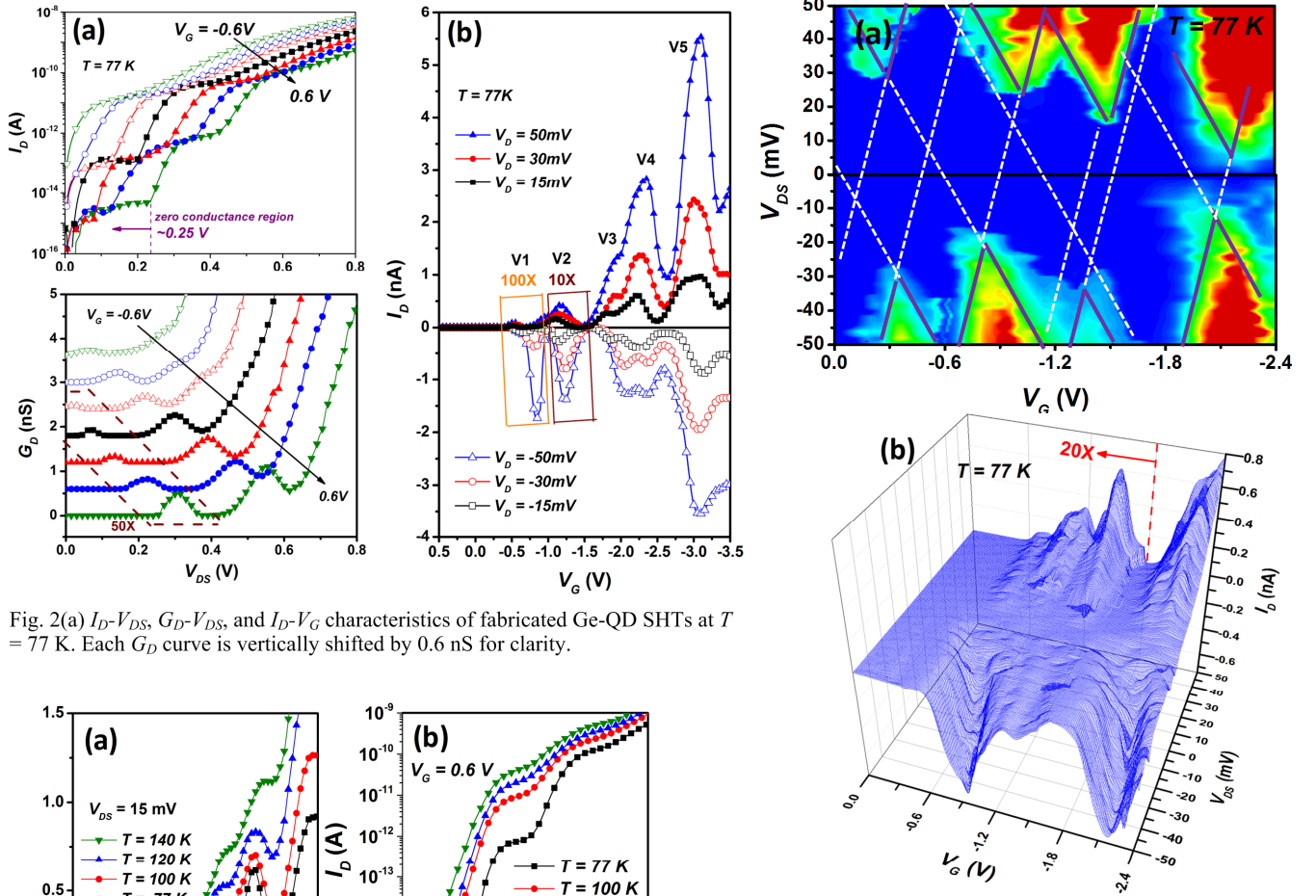


Fig. 2(a) I_D - V_{DS} , G_D - V_{DS} , and I_D - V_G characteristics of fabricated Ge-QD SHTs at $T = 77$ K. Each G_D curve is vertically shifted by 0.6 nS for clarity.

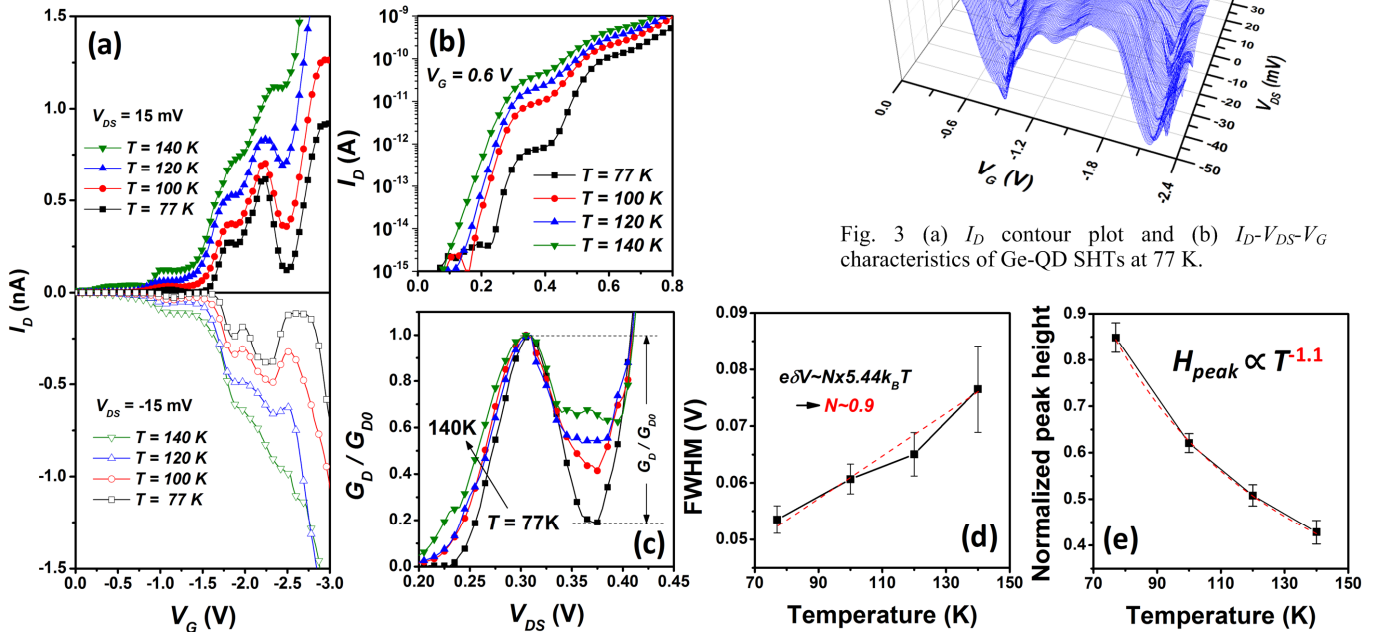


Fig. 4(a) I_D - V_G , (b) I_D - V_{DS} , and (c) G_D/G_{D0} - V_{DS} characteristics of fabricated Ge-QD SHTs at $T = 77$ -140 K. (d)/(e) Temperature dependence of the G_D peak FWHM and Height.