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Sub-Milliwatt, 30-GHz Microprocessor Based on Low-Voltage Rapid Single-Flux-Quantum Circuit Technology

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Abstract

We report high-speed operation of low-power microprocessor prototype based on the low-voltage rapid single-flux-quantum (LV-RSFQ) circuit technology using superconductor devices. When a supply voltage is lowered, both static and dynamic energy consumption in RSFQ circuits are reduced, in exchange for slower switching speed. We optimized the supply voltage for most energy-efficient operation, and improved the energy-delay product (EDP) to one fifteenth of the previous design with the help of an advanced fabrication technology. The designed microprocessor operated at a clock frequency of 30 GHz with power consumption of 0.23 mW.

1. Introduction

Energy-efficiency is a technical challenge for high-end computing systems such as exascale computing. The superconducting rapid single-flux-quantum (RSFQ) logic [1] is a promising technology for ultralow-energy digital integrated circuits based on a different physics. The typical operation frequency of RSFQ circuits exceeds several tens of gigahertz, while power consumption is only a few microwatts per gate. Many RSFQ LSIs composed of thousands of Josephson Junctions (JJs) have been successfully demonstrated, including simple microprocessors [2-3].

The intrinsic energy consumption of a switching event in RSFQ gates is only $I_C\Phi_0$, where I_C and Φ_0 are the Josephson critical current and magnetic flux quantum, respectively. The conventional RSFQ circuits actually consume much larger static energy at resistors to supply constant dc power currents (bias currents). The resultant ~100 aJ/gate energy consumption is still extremely small compared to semiconductor devices; however, this reduces the energy efficiency of RSFQ circuits, especially when the 4.2-K cooling energy of systems is taken into account. Recently, several studies for reducing/eliminating the static energy consumption in RSFQ circuits have been reported, such as inductive-biasing technique [4-5], reciprocal quantum logic [6], ERSFQ/eSFQ circuit families [7-8], and adiabatic quantum flux parametrons [9].

In this paper, we report high-speed operations of low-power microprocessor prototype based on the low-voltage RSFQ (LV-RSFQ) circuit technology [10]. Our approach is to drive conventional RSFQ circuits with lowered constant dc power voltages. The purpose of this study is to prove its effectiveness for large-scale, complicated digital circuits. Here we briefly introduce the LV-RSFQ circuit, and describe the design of the low-power microprocessor. We report the experimental results of the on-chip high-speed tests of the fabricated chips.

2. Circuit Design

In the conventional RSFQ circuit design, a sufficiently-high bias voltage for the voltage drop across a JJ is selected to provide constant driving currents to JJs. Namely, typical bias voltage is ~10 I_CR_S (product of the critical current and the value of the shunt resistor), and large amount of energy is statically consumed by the bias feed resistors.

In the LV-RSFQ circuit, we feed bias currents to circuits from lowered constant voltage sources through small resistors. Both static and dynamic energy consumption are reduced because of the suppression of the amplitudes of voltage pulses across Josephson junctions, in exchange for slower switching speed. Figure 1 shows the energy-delay product (EDP) of the LV-RSFQ shift registers [10]. The most energy-efficient bias voltage in LV-RSFQ ranges from 0.1 to 1.0 I_CR_S, and the switching speed is improved by the fabrication technology with a higher critical current density J_C.

We designed a microprocessor based on the previous design [2], and refined for the 10-kA/cm^2 Nb/AlO$_x$/Nb fabrication process with nine metal layers [11]. The microprocessor has a simple, bit-serial microarchitecture with 8-bit-wide instructions and data. The instruction set is composed of seven instructions essential for a microprocessor including memory access, register operations, and program controls (conditional branches, etc.). The major components of the microprocessor are a controller, a 5-bit program counter, an 8-bit instruction register, two 8-bit registers and a bit-serial ALU. Memories were not implemented. Instead, several shift registers were integrated to support on-chip high-speed testing.

In comparison to the previous design, the number of Josephson junction and circuit area were reduced by 23% and 50%, respectively, because of introduction of the multi-layered fabrication process, where interconnects of passive transmission lines were formed on the dedicated layers underneath logic gates. The designed bias voltage was 0.5 mV (0.44 I_CR_S), which is 1/5 of our conventional RSFQ

design. We estimated that the increase in the critical current density leaded to doubled operating frequencies. The target operating frequency is 30 GHz for bit-serial operating. The total power consumption was estimated to be 15% of the previous design, and the energy-delay product (EDP), which indicates a balance between competing circuit performance metrics of energy efficiency and speed, was improved approximately 15 times.

3. Experiment

Figure 2 displays a microphotograph of the designed microprocessor chip. The circuit was composed of 3869 JJs, and occupied an area of 1.38 mm × 1.71 mm.

The functionality of the microprocessor was tested using high-speed clock signals generated by the on-chip built-in clock generator. We confirmed the correct operation of the microprocessor up to 30 GHz. Figure 3 shows one example of test results, where the microprocessor loaded data, performed two register operations, and stored the result by a sequence of four instructions.

The total power consumption including the components for on-chip high-speed testing and estimated performance were 0.23 mW, and 400 million instructions per second (MIPS). Although the functionality is poor, the performance-to-power ratio ranges from five to six orders of magnitude higher than those of conventional CMOS microprocessors.

4. Conclusions

We report high-speed operation of low-power microprocessor prototype based on the low-voltage rapid single-flux-quantum (LV-RSFQ) circuit technology using superconductor devices. We optimized the supply voltage for most energy-efficient operation, and improved the energy-delay product (EDP) to one fifteenth from the previous design, with the help of an advanced fabrication technology. We confirmed that the designed microprocessor operated at a clock frequency of 30 GHz with power consumption of 0.23 mW. The results indicated the effectiveness of LV-RSFQ circuit technology for large-scale, complicated circuits.

Acknowledgements

The circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2). The AIST-ADP2 is based on the Nb circuit fabrication process developed in International Superconductivity Technology Center (ISTEC). This work was supported by KAKENHI (22226009, 24760276), ALCA-JST, and by VLSI Design and Education Center(VDEC), The University of Tokyo with the collaboration with Cadence Corporation.

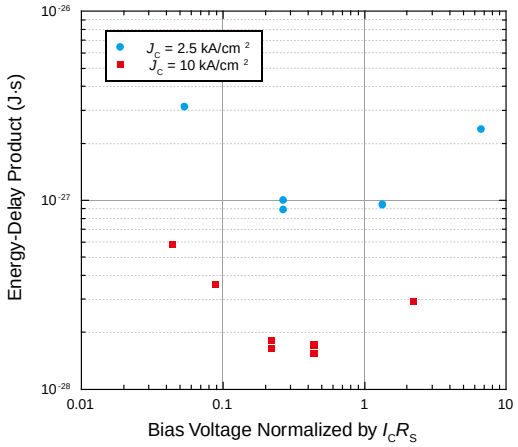

Fig. 1 Energy-delay product of LV-RSFQ shift registers [10]

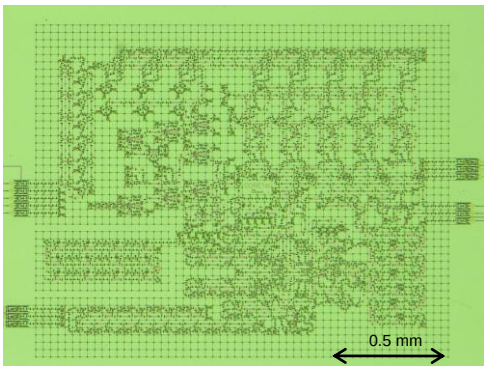

Fig. 2 Microphotograph of LV-RSFQ microprocessor.

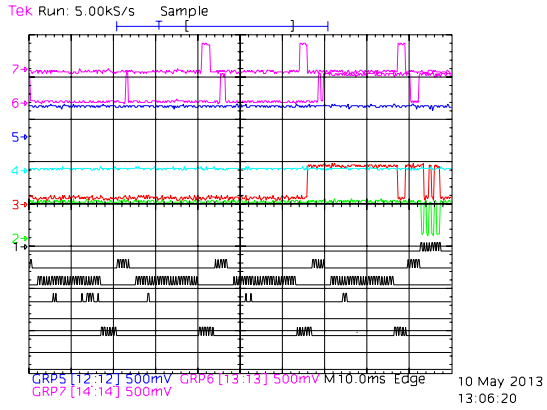

Fig. 3 Test result of LOAD, ADD, and STORE instructions.

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