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Peak Position Control of Coulomb Oscillations in Silicon Single-Electron Transistors with Floating Gate Operating at Room Temperature

Yuma Tanahashi[1,2], Ryota Suzuki[1], Takuya Saraya[1], Toshiro Hiramoto[1]
[1]Institute of Industrial Science, The University of Tokyo, [2]Chuo University
4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan, Phone: +81-3-5452-6264, E-mail: yuma@nano.iis.u-tokyo.ac.jp

Abstract

Silicon single-electron transistor (SET) with a floating gate (FG) that covers the entire SET structure is fabricated and the parallel peak control without the peak height change is demonstrated at room temperature. The proposed FG SET is suitable for adding more functionality into CMOS.

1. Introduction

A silicon-based SET operating at room temperature is one of the promising device elements for future high density and functional VLSIs thanks to its unique feature of Coulomb blockade oscillations [1-7]. As an application of silicon SETs integrated into CMOS VLSIs, we already proposed an analog pattern matching circuit using SETs [5] and demonstrated successful operation of analog pattern matching at room temperature. One of the key features that realized the analog pattern matching was the "non-volatile memory effect" in silicon SETs. The silicon SETs had nanocrystal FG to control the potential of silicon quantum dots, and the peak of Coulomb blockade oscillations can be shifted in a non-volatile manner [3,5], which add more functionalities to SETs and CMOS circuits.

However, the nanocrystal FG SETs has a disadvantage. The peak height of Coulomb blockade oscillations is changed when the peak is shifted by the write voltage application to the control gate [3,5]. Therefore, the control of the peak shift is also necessary after the peak shift control, which is a significant overhead for circuit applications. This peak height change may be caused by very local charge injections to nanocrystal FG that leads to local potential change instead of overall potential change.

In this study, a SET with a FG that covers entire SET structure is fabricated in order to prevent the peak height change by the charge injection to FG. The peak shift of the Coulomb blockade oscillations without the peak height change is successfully demonstrated at room temperature.

2. Device Structure and Fabrication

Fig. 1 shows schematics of device structures of FG SETs. Fig.1(a) is the nanocrystal FG SET [3,5] where one of the tunneling barriers is raised more than the others by the local charge injection into a nanocrystal, leading to the peak height change after the peak shift. Fig.1(b) shows the device structure with a FG proposed in this study. Since FG covers the entire SET, the potential of the dot and barriers are equally raised by the charge injection into FG.

The fabrication process of SET is based on the previous studies in our group [6]. First, SOI layer of SET channel region is selectively thinned to less than 5nm by LOCOS process, while the SOI layer of source/drain regions remain thick to suppress parasitic resistance. The BOX thickness is 200nm. The SET channel is composed of an ultra-narrow nanowire structure patterned by EB lithography and dry etching. A small dot with size of less than 5nm is naturally formed and the device acts as a SET [6]. SET has two poly Si layers (control gate and FG) separated by a 27nm-thick oxide layer. The thin gate oxide below FG is 9nm-thick, which acts as a tunneling oxide.

The disadvantage of a FG against the nanocrystal FG is the short retention time of non-volatile memory effect. To solve this problem, additional oxidation is performed after the dry etching of the gate stack to thicken the edge of the tunneling oxide.

3. Results

Figs. 2 and 3 show I-V characteristics of two SETs (SET-A and SET-B) at room temperature. SET-A shows two peaks of Coulomb blockade oscillations and SET-B shows a clear peak of peak-to-valley-ratio (PTVR) of 14.1.

Figs. 4 and 5 show the peak shift of the oscillations after the application of write voltage (V_{write}) of 5V for various periods of time. Before V_{write} application, the erase voltage of -3.2V is applied each time and the peak is returned back to the initial position. The parallel shifts of the Coulomb blockade oscillations without the change of the peak heights and peak shapes are successfully achieved. This is because FG covers the entire SET structure and the potential of the quantum dot and tunnel barriers are equally raised.

Figs. 6 and 7 shows Vth shift (ΔVg) as a function of the write time. ΔVg increases as the wirte time increases, indicating the precise ΔVg control is possible by controlling the write time. Fig. 8 shows retention characteristics of the non-volatile peak shift behavior. The peak position just after the shift remains after 7 days and hence the retention time is long enough. These results indicate that the FG SET proposed in this study is suitable for the applications for adding more functionality into CMOS.

4. Conclusions

SET with a FG covering the entire SET structure, instead of nanocrystal FG, is fabricated and the peak shift without the change in peak height and peak shape is demonstrated at room temperature.

Acknowledgements

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References

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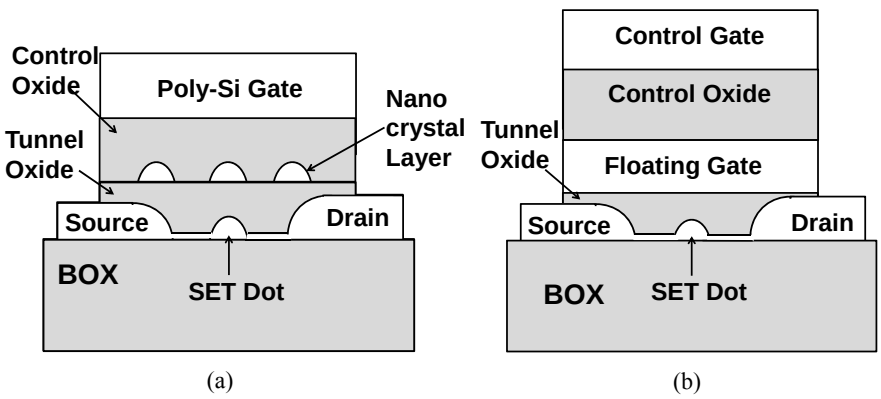

Fig.1. Schematics of silicon SETs with floating gates. (a) A nanocrystal floating gate SET studied in Ref [5]. (b) A floating gate SET proposed in this study.

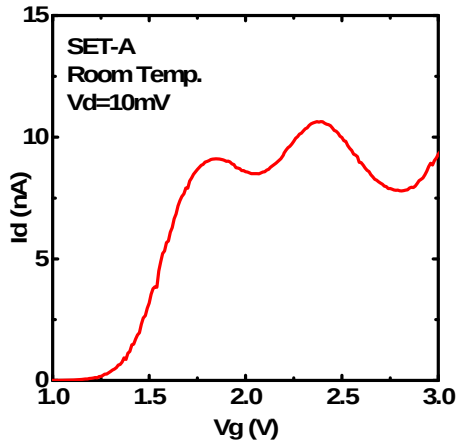

Fig.2. I-V characteristics of SET-A at room temperature. Two peaks of the Coulomb blockade oscillations are observed.

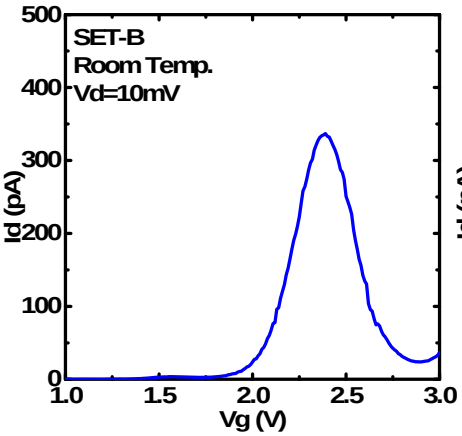

Fig.3. I-V characteristics of SET-B at room temperature. A clear Coulomb blockade oscillation peak with PTVR of 14.1 is observed.

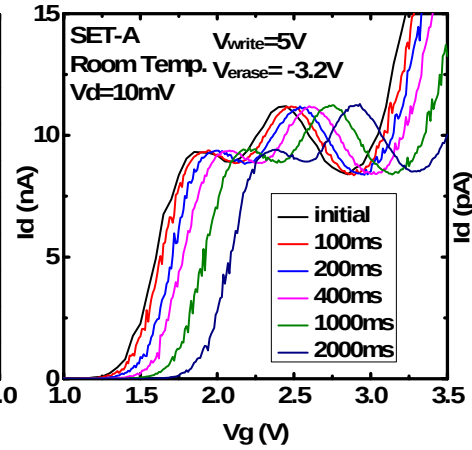

Fig.4. Peak position control in SET-A with Vwrite = 5V. The write time is varied from 100ms to 2s. Clear peak shift is observed.

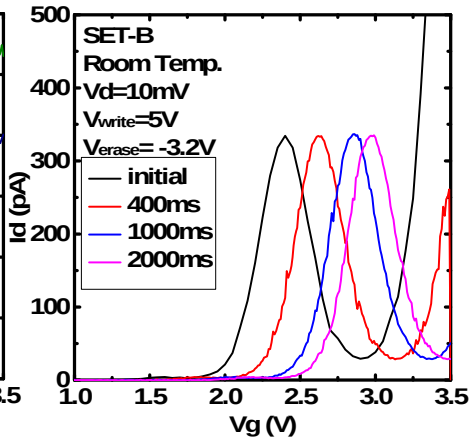

Fig.5. Peak position control in SET-B with Vwrite = 5V. The write time is varied from 400ms to 2s. Clear peak shift is observed.

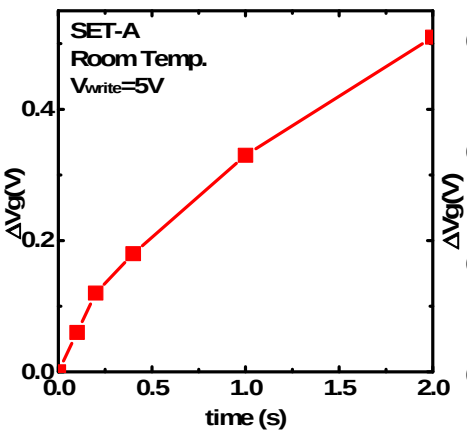

Fig.6. Peak position shift (ΔVg) as a function of write time in SET-A. The peak position can be precisely controlled by changing the write time.

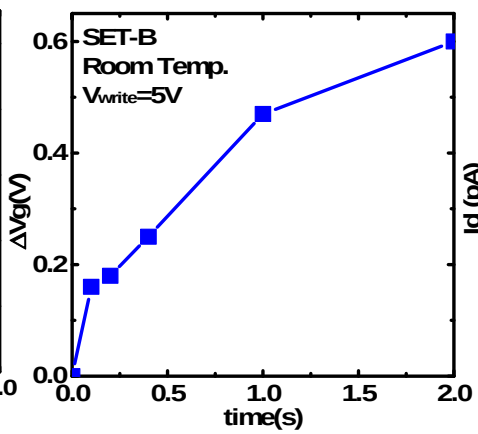

Fig.7. Peak position shift (ΔVg) as a function of write time in SET-B. The peak position can be precisely controlled by changing the write time.

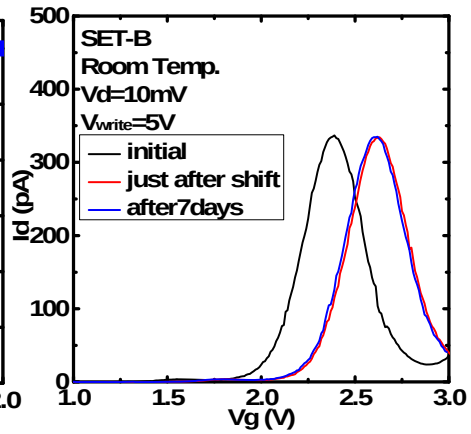

Fig.8. Retention characteristics of SET-B. The shifted I-V curve is almost unchanged after 7 days.