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G-6-3

Polarity Dependence on Electrical Properties of Low-k Dielectric in Copper Interconnect Structures

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Introduction

A thorough investigation of electric properties of low-k dielectric becomes very important for advanced microelectronic devices. We characterized the conduction and capacitance properties of inter and intra level carbon-doped silicon oxide (SiOCH) low-k dielectric at different temperatures and bias polarities. Effects of structure and stress on current were investigated. Electrical breakdown fields (Ebd) were measured as a reliability index and also show bias polarity dependence. Capacitors with Cu and low-k dielectric must be as stable as possible with respect to voltage and temperature. We demonstrated the novel voltage dependence on the capacitance of low-k structures due to temperature and injection current with bias polarity.

Experimental

Inter and intra level Cu comb structures were fabricated on 300 mm wafers using 45 nm Cu/SiOCH low-k dual damascene processes. Cu lines were electroplated into dielectric trenches with TaN/Ta liners and capped with SiCN layer (Fig. 1). The leakage current and capacitances of low-k dielectric were measured at various temperatures from 25 to 250 °C. Positive voltages were applied at up level metal lines (bias up) or low level metal lines (bias down) for inter level structures.

Results and Discussions

Fig. 2 (a) shows the bias polarity dependence of the leakage current of inter level structure. The bias up currents are higher than bias down currents. At lower electric fields, all leakage currents follow Ohmic conduction (Fig. 2 (b), Eq. (2) of Fig. 3). At higher electric field, intra level and bias up inter level current follow Poole-Frenkel (PF) conduction (Eq. (2) of Fig. 3), with trap barrier height of 1.07 eV (Fig. 4(a)). Current under bias down condition at higher field shows Fowler-Nordheim (FN) conduction (Eq. (3) of Fig. 3) with barrier height Φ_{FN} of 2.5 eV (Fig. 4(b)). The conduction mechanism for intra level and inter level bias up condition is proposed to be field assistant excitation of trapped electrons with low Schottky barrier and high surface defect states (Fig. 5 (a)). On bias down condition, FN tunneling with higher barrier dominates at high field (Fig. 5 (b)). FEM analysis shows the maximum electric field locates at the triple point (Fig. 6(a)) of intra level structure, where large defect density exists. The current density of intra level structure, therefore, is larger than those of inter level structure (Fig. 7(a)). The leakage current of Cu structure without liner is report to be smaller than that with TaN/Ta liner (Fig. 7(b)) [1]. The location of maximum electric field of liner free structure changed to at low-k portion (Fig. 6(b)). The leakage conduction then change to FN emission. The mechanical stress and defect density induced of SiCN between Cu lines is shown to be reduced for liner free interconnect (Fig. 8). Both above effects explain the smaller leakage current of liner free interconnect structure.

Fig. 9 shows the Ebd results of different bias conditions. The bias condition with smaller leakage has larger breakdown field. The Ebd results indicate the conduction current driving breakdown model [1] is appropriate for low-k structure instead of thermochemical E model.

The relative capacitance versus voltage (C-V) characteristics of inter level stack structure were measured at different temperature (Fig. 10(a)). On this bias condition, low-k and Cap SiCN dielectrics are connected in series (Fig.1(a)). The nonlinear C-V curves are concave downward at low temperature and turn into concave upward at high temperature. The C-V results demonstrate the voltage nonlinearity of low-k material, describe by

$$\Delta C / C_o = (C(V) - C_o) / C_o = \alpha V^2 + \beta V \ , \qquad (1)$$

where Co is the capacitance at zero bias, α and β are the quadratic and linear voltage coefficient of capacitance (VCC) respectively. Fig. 11(a) shows α increases linearly as temperature increases. The leakage current of inter level structure is very small (Fig. 2(a)) at low temperature and the maximum field is located at low-k dielectric (Fig. 11(b)). The concave downward C-V curves of inter level capacitance at low temperature can be explained by the dipole orientation polarization model (Eq. (4) of Fig. 3) [2]. At higher temperature, the dipole polarization effect reduces and the leakage current increases. The carrier injection model then can be applied for such concave upward C-V curve (Eq. (5) of Fig. 3) [3]. The relative C-V curves of intra level low-k structure with the largest leakage current (Fig. 7(a)) show concave upward at both low and high temperatures (Fig. 10(b)). The carrier injection model applied for intra level capacitance. The linearity of VCC usually can be improved by using a stack insulator structure with different VCC dielectrics. Our results demonstrate such VCC improvement by two-layer stack capacitor should consider the temperature effect for accuracy requirement.

Conclusions

Novel polarity dependences of conduction currents and breakdown voltages were found. This polarity dependence of conduction is explained by the different carrier barriers and defect states on the different surfaces. The results of dielectric breakdown fields are consistent with current conduction results. Voltage dependence of capacitances of Cu/low-k materials are investigated and show temperature and bias polarity dependence. The orientation polarization and space charge polarization model apply to the low-k dielectric structures at different bias and temperature conditions accordingly.

References

[1] F. Chen, et al., IRPS., 2012, pp. 3A.3.1-9.
[2] T. H. Phung, et al., IEEE EDL, vol. 32, p. 1671, 2011
[3] S. Blonkowski, APL vol. 91, p. 172903, 2007.

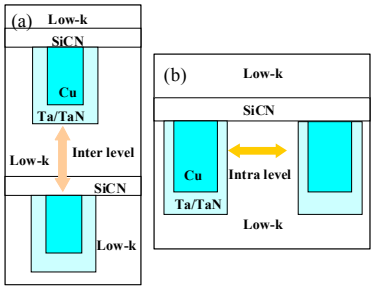

Fig. 1. (a) Inter and (b) intra level Cu structure with low-k dielectric for capacitance and conduction measurements.

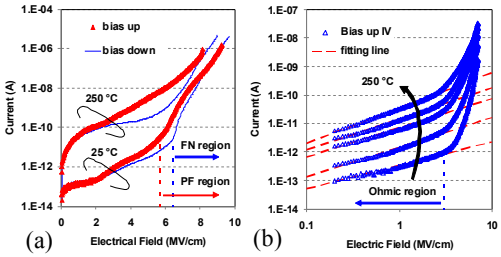

Fig. 2. (a) Leakage current vs. electrical field for inter level low-k structure under different temperatures and voltage bias conditions. (b) Low field leakage current vs. bias up electrical field for inter level low-k structure at different temperatures.

$$\text{Ohmic}: J \propto E\exp(-E_a/kT) \quad (1)$$

$$\text{PF}: J \propto E\exp(-q(\varphi_{PF}-\sqrt{qE/\pi\varepsilon_i})/kT) \quad (2)$$

$$\text{FN}: J \propto E^2\exp(-8\pi\sqrt{2m^*}(q\varphi_{FN})^{3/2}/3qhE) \quad (3)$$

$$\Delta C/C_o = = [L(a)/a - 1/3]N_b\mu_b 2/\varepsilon(0)kT \quad (4)$$

$$C = \text{Real}(\frac{\varepsilon(1+j\omega\tau)/d}{j\omega\tau+\tanh(A)/A}) \quad (5)$$

Fig.3. (1) Ohmic conductions, (2) Poole-Frenkel conductions, (3) Fowler-Nordheim conductions, (4) dipole orientation polarization capacitance, and (5) space charge polarization capacitance.

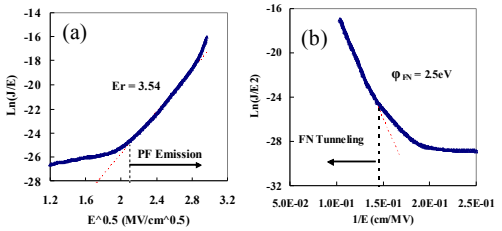

Fig. 4. High field inter level conductions: (a) Plot of Ln(J/E) vs E^0.5 showing Poole-Frenkel emission on the bias up condition. (b) Plot of Ln(J/E2) vs 1/E showing Fowler-Nordheim tunneling on the bias down condition.

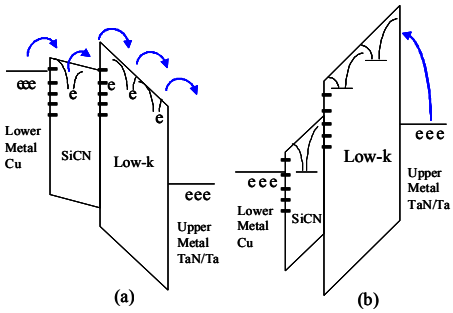

Fig.5. Energy diagrams: (a) Poole-Frenkel emission at high field on bias up condition. (b) Small conduction current on bias down condition due to higher barrier energy until Fowler-Nordheim tunneling dominates at high field.

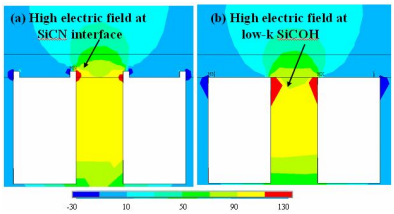

Fig. 6. FEM electrical field contour of intra level structures (a) with liner and (b) without liner.

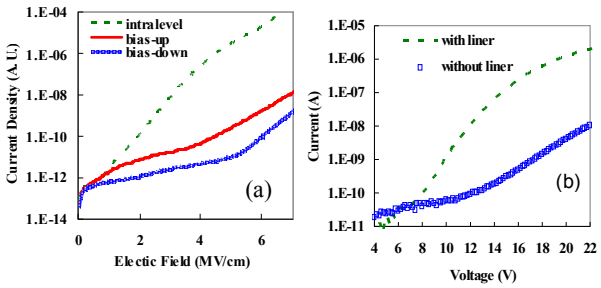

Fig. 7. (a) Leakage current density vs. electrical field for intra and inter level (bias up and down) low-k structures. (b) Intra level I-V characteristics of Cu structues with and without liner.

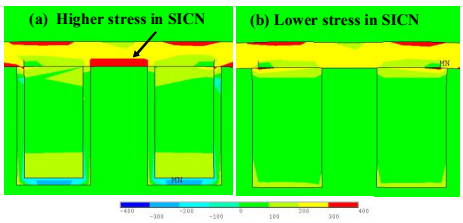

Fig. 8. FEM stress contours for Cu structures (a) with liner and (b) without liner.

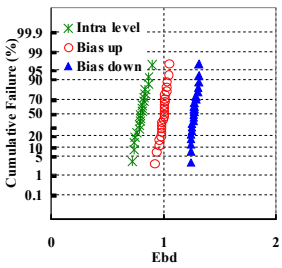

Fig. 9. Normalized breakdown field distributions for intra and inter level bias conditions.

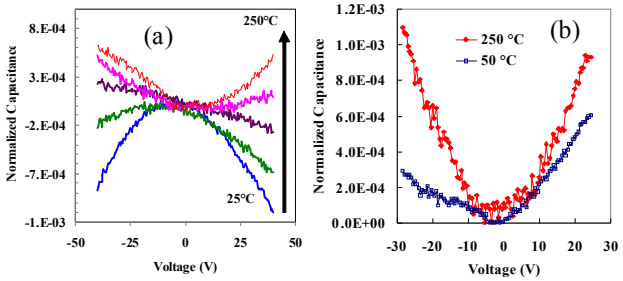

Fig. 10. Normalized (a) inter and (b) intra level C-V curves at different temperatures.

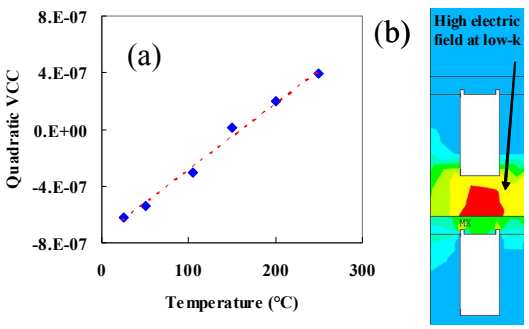

Fig. 11. (a) Temperature dependence of quadratic VCC of inter level low-k capacitance (b) FEM electrical field contour for inter level structure.