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Local Bending Stress Reduction with Room-Temperature Curing Adhesive for Decrease in Keep-out-Zone (KOZ) of 3D IC

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1. Introduction

Three-dimensional IC (3D IC) has attracted much attention as a promising method to enhance performance of IC [1]. Recently, great interests in electrical and mechanical reliability issues are increasing among 3D IC researches for production of 3D IC [2,3]. Conventional 3D ICs consist of vertically stacked several thin IC chips with lots of through-Si vias (TSVs) and metal microbumps that electrically connect both upper and lower LSI chips. Metal microbumps are surrounded by organic adhesive called underfill material. Generally, coefficient of thermal expansion (CTE) of the underfill material is larger than that of metal microbumps. As shown in Fig.1, this CTE mismatch induces local bending stress in thinned Si chips/substrates. In addition, this local bending stress would affect MOSFET performance in thinned Si chips [4]. One of the causes of this issue is temperature change due to cooling after heat curing. Therefore, we propose to use low temperature curing adhesive to suppress the temperature change. In this paper, we have evaluated the effect of low-temperature curing adhesive on the local bending stress by measuring surface profile and change of *I-V* characteristics before and after underfill process.

2. Experimental

Figurer 2 shows a schematic cross-section of test structure to evaluate the effects of local bending stress. The test structure is composed of Si (dummy) microbumps, an organic adhesive, and a thinned Si chip stacked on Si substrate. This test structure can generate the controlled local bending stress in a thinned chip on Si microbumps, and it enables us to evaluate only local bending stress due to the CTE mismatch between organic adhesive and Si microbumps. The test structure was fabricated with following processes, as shown in Fig.3. First, Si microbumps were formed on the Si substrate by inductively coupled plasma reactive ion etching (ICP-RIE). The bump size and height were 20 μm by 20 μm and 20 μm. The bump pitches were 50, 100, 300, and 500 μm. Then, the thinned Si chips were bonded on the Si substrate which was coated with an adhesive A. In this paper, the thinned chip thickness was 35 μm. After that, two kinds of epoxy resin were additionally coated around the thinned chips depicted as the adhesive B in Fig. 3. Here, one resin was a heat curing type, and the other was a room-temperature curing type. The chip and the Si substrate were temporarily exposed in vacuum atmosphere and opened to the air to completely fill gaps between the thinned chip and the substrates by the epoxy. Finally, the heat curing epoxy resin was cured at 190 degree C for 1 hour, and the room-temperature epoxy resin was held at room temperature. In general, the procedures after second step were called underfill process. This structure can give a tensile stress of more than 1 GPa to thinned Si chip using heat curing resin [5]. After underfill process, we measured the surface profile and the I_d-V_d characteristics of nMOSFET fabricated on the locally-bended thin Si chip.

3. Results and discussion

Figure 4 shows the results of surface profile measurements of thinned Si chips stacked on the substrates with the Si microbumps. Here, a deflection is a height difference of the surface of bended Si chip. The deflection of the chip increases with an increase in the Si microbump pitch. In other word, fine-pitch microbumps (high-density microbumps) can provide smaller bending of the chip. It was clearly observed that the deflection using heat curing adhesive was approximately three times larger than the deflection using the room-temperature curing adhesive. Figure 5 shows I_d-V_d characteristics of nMOSFETs with L_g/W_g of 0.5 μm/10 μm in thinned Si chips before and after underfill process. The nMOSFET was located at 15-μm away from the center of the nearest Si microbump. With the heat curing adhesive, the drain current increased by the local bending stress. Meanwhile, the drain current didn't change with the room temperature curing adhesive. These results indicated that the room-temperature curing adhesive was one of the most effective to suppress the chip local bending.

In addition, these results demonstrated that using room-temperature curing adhesive reduced a keep-out-zone (KOZ) that transistors should not be placed, as shown in Fig. 6. KOZ is defined by the area where Si strain is more than specified value. It is well known in mechanics of materials that the strain is proportional to d^2Y/dX^2. Here, Y is a displacement perpendicular to Si chip surface, and X is a displacement in parallel with Si chip surface. By using room-temperature curing adhesive, d^2Y/dX^2 totally decreased in accordance with decreases of the Si-chip deflection, as shown in Fig. 4. Therefore, the room-temperature curing adhesive reduces the KOZ, and enlarges the area where the transistors can be freely placed.

4. Conclusion

The effects of local bending stress applied to the thinned Si chips were investigated in detail with the unique test structure that can generate controlled local bending stress by the CTE mismatch between organic adhesive and Si microbumps. The local bending stress affected the *I-V* characteristics of MOSFET. It was obviously clarified that the room-temperature curing adhesive can suppress the local bending of the thinned Si chip. In order to realize higher performance 3D IC with diminished circuit performance degradation and fluctuation, careful transistor layout and process design including choice of the underfill material were strongly required.

Acknowledgments

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References

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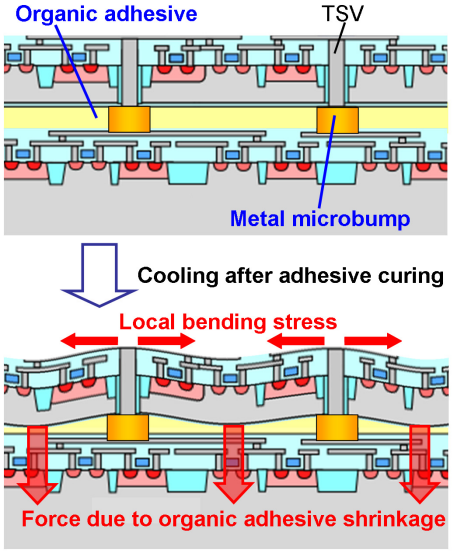

Fig. 1. Schematic cross-section of 3D IC expressing local bending stress due to the CTE mismatch between organic adhesive and metal microbump.

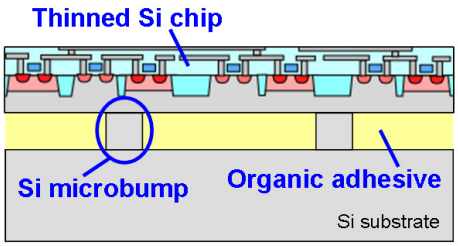

Fig. 2. Schematic image of the test structure to evaluate the effect of controlled local bending stress due to CTE mismatch between microbump and organic adhesive.

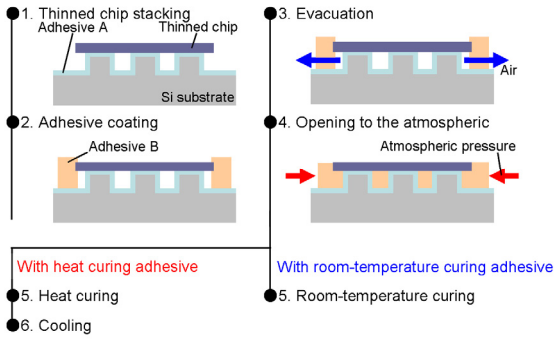

Fig. 3. Process flow of the test structure fabrication. (Underfill process consists of procedures after second step.)

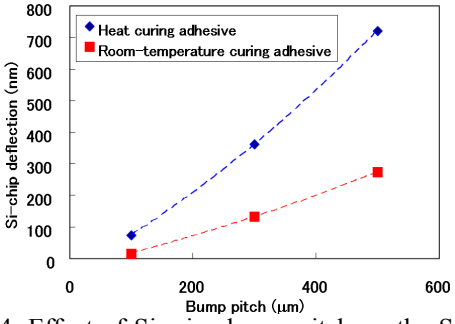

Fig. 4. Effect of Si-microbump pitch on the Si-chip deflection for two types of adhesives.

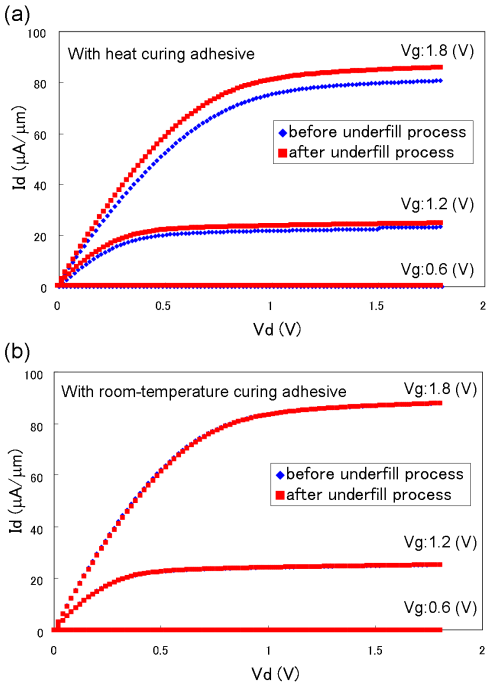

Fig. 5. Id-Vd characteristics of nMOSFET on thinned Si chip with (a) heat curing adhesive, and (b) room-temperature curing adhesive.

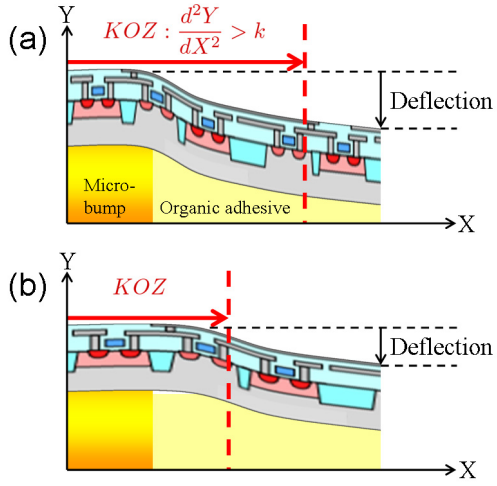

Fig. 6. KOZ around microbump with (a) heat curing adhesive and (b) room-temperature curing adhesive.