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A CMOS Image Sensor Using Column-Parallel Forward Noise-Canceling Circuitry

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Abstract

This paper presents a CMOS image sensor using column-parallel forward noise-canceling circuitry (FNC) for noise reduction of the pixel readout chain. A proposed FNC has been developed to provide a sharp noise-filtering in order to suppress both random noise and temporal line noise. The readout architecture consists of a high-gain amplifier with correlated-double-sampling, a FNC, and sample-and-hold circuits. A prototype $400^H \times 250^V$ CMOS image sensor has been fabricated in a 0.18 μm 1-Poly 3-Metal CMOS technology with pinned-photodiodes. The measured input-referred noise of the signal readout chain is 65 μV_{rms}, which has been reduced by 24 % compared to that of the conventional readout architecture.

1. Introduction

In CMOS image sensors (CIS), photo signals are read out through a pixel readout chain, consisting of a pixel circuit and a readout circuitry. A column-parallel signal readout chain using the correlated-double-sampling (CDS) operation is widely employed to remove pixel-related kTC noise and fixed pattern noise [1]. In a conventional readout circuitry [2-4], a high-gain column amplifier placed in front of column sample-and-hold (S/H) circuits is utilized to increase photo signal sensitivity and suppress the random noise of output buffers and quantization noise of an analog-to-digital converter (ADC). In Fig.1, compared with a conventional pixel readout chain, a new pixel readout chain using a forward noise-canceling circuitry has been realized to provide a shape noise-filtering for further reduction of random noise as well as temporal line noise.

2. Signal Chain with Forward Noise-canceling Circuitry

Figure 2 shows the concept of the proposed forward noise-canceling circuitry (FNC). The required signal from the pixel readout output is a constant voltage but the temporal noise superposed on the signal includes 1/f noise, random telegraph noise, and thermal noise arising from the pixel readout circuitry. A FNC is composed of a forward path and a feed-through path. Employing a high-pass filter in the forward path, the high-frequency temporal noise (V_{HPF}) of the input voltage is extracted. Next, the reverse-phase voltage (V_{FNC}) of V_{HPF} is generated through an inverting amplifier. On the other hand, an in-phase voltage is generated in the feed-through path. Eventually, output signals of the two paths are summarized to acquire the required noise-canceling signal (V_{OUT}) with a significant reduction of both the random noise and temporal line noise.

In Fig.3, it shows the conceptual and implemented schemes of the FNC. In the conceptual scheme, a source follower and a common source amplifier are utilized to implement a non-inverting amplifier and an inverting amplifier, respectively. The implemented FNC is a circuit combination of a source follower and a common source amplifier with a MOS-based RC high-pass filer. The resistance is variable through the adjustment of V_G, which is employed to control the corner frequency (f_{3dB}) of the high-pass filter, i.e. the noise-canceling bandwidth.

Figure 4 shows the dual-gain mode pixel readout chains using a forward noise-canceling circuitry. A two-shared pixel design is employed. The readout chains of high-gain mode and low-gain mode are for a high-sensitivity output and a high-dynamic range output, respectively [4].

3.Experimental Results

A prototype CMOS image sensor has been fabricated in a 0.18 μm 1-Poly 3-Metal CMOS process with pinned photodiodes. The chip micrograph is shown in Fig. 5. A $400^H \times 250^V$ pixel array and the column-parallel readout circuitry using the FNC were implemented on 2.5 mm × 2.5 mm die. Both the pixel pitch and column circuit pitch were 4.5 μm. Figure 6 shows the measured input-referred noise (refer to V_{FD}) of the high-gain column readout chain and high-gain pixel readout chain (pixel source follower with the high-gain readout chain), respectively. As V_G increases, the resistance of M_{RES} becomes increasing, which results in more noise-canceling at higher frequency. The minimum noise of the high-gain column readout chain is 38 μV_{rms} (at V_G= 1V). The noise of the conventional and new readout architecture is 86 μV_{rms} and 65 μV_{rms} (at V_G= 1V), respectively. The new readout chain reveals a noise reduction of 24 % compared to the conventional one. In Fig. 7, it shows the photoelectric conversion characteristics of the dual-gain mode (a combination of high-gain and low-gain modes). Figure 8 shows the sample images of high-gain mode, low-gain mode and dual-gain mode, respectively. Table I shows the measurement summary.

4. Conclusions

A CMOS image sensor using the column-parallel FNC has been demonstrated. The concept of the FNC and the implemented FNC scheme have been introduced. Benefiting from its significant noise reduction, a low-noise readout chain for a pixel array can be achieved.

References

[1] H. Takahashi et al., *ISSCC* (2007) 510.
[2] S. Kawahito et al., *ISSCC* (2003) 224.
[3] K. B. Cho et al., *Int. Image Sensor Workshop* (2007) 55.
[4] P. Vu et al., *Int. Image Sensor Workshop* (2011) P35.

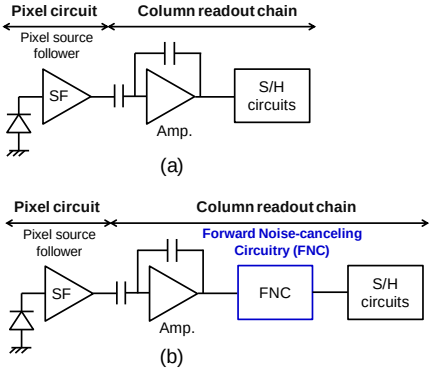

Fig. 1 Pixel readout chain. (a) conventional. (b) proposed.

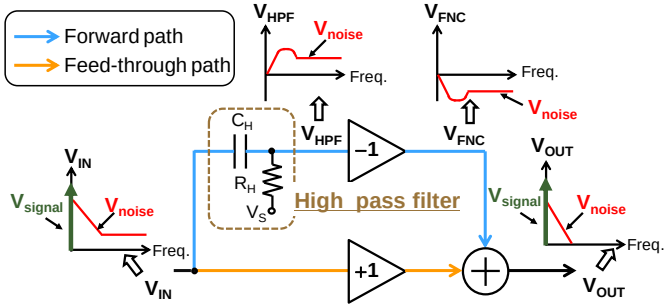

Fig. 2 Concept of the proposed forward noise-canceling circuitry.

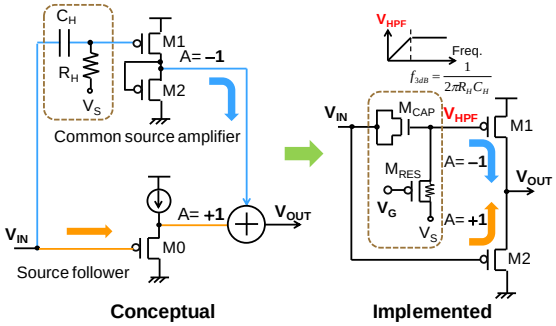

Fig. 3 Conceptual and implemented schemes of the FNC.

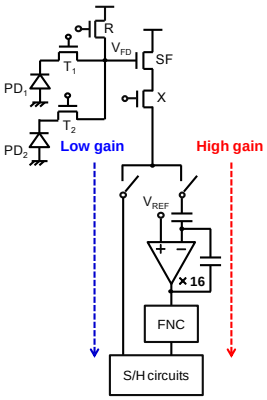

Fig. 4 Dual-gain mode pixel readout chains using a FNC.

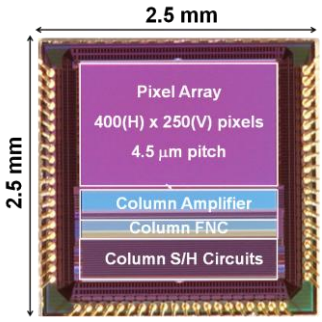

Fig. 5 Chip micrograph.

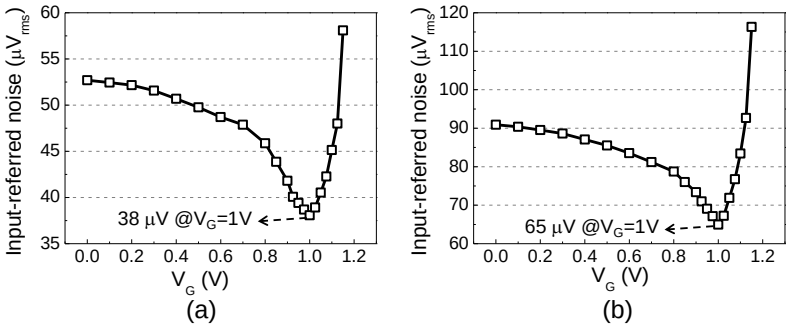

Fig. 6 Input-referred noise (refer to V_{FD}). (a) high-gain column readout chain. (b) high-gain pixel readout chain.

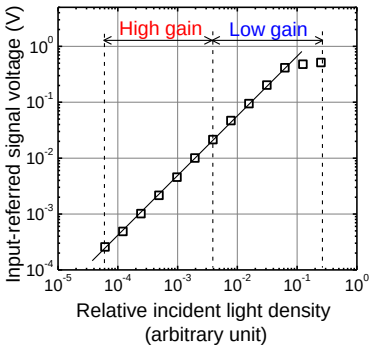

Fig. 7 photoelectric conversion characteristics of a combination of high-gain and low-gain modes

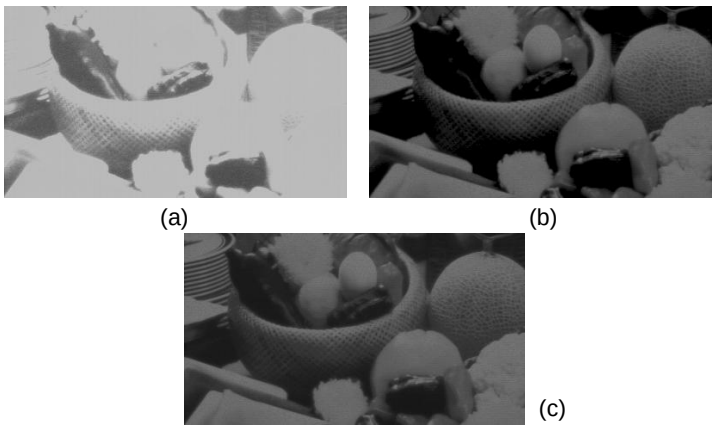

Fig. 8 Sample images (F number= 4.0, exposure time= 16.4 ms). (a) high-gain. (b) low-gain. (c) dual-gain mode.

Table I Measurement summary

Process technology	0.18 μm 1P3M CMOS technology with pinned-photodiodes
Die size	2.5 mm × 2.5 mm
Number of total pixels	$400^H \times 250^V$
Number of effective pixels	$400^H \times 226^V$
Pixel / column circuitry pitch	4.5 μm / 4.5 μm
Conversion gain	68 μV / e^-
Dynamic range	66 dB
Input-referred noise of column readout chain	38 μV_{rms}
Input-referred noise of overall readout architecture	65 μV_{rms}