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A CMOS Image Sensor with High-speed Pixel-parallel Pipelined Readout Channels for Multi-point Fluorescence Correlation Spectroscopy

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Abstract

A high-speed CMOS image sensor aiming at 1MS/s continuous data acquisition for multi-point fluorescence correlation spectroscopy is proposed, which is based on complete parallel and multi-channel pipelined pixel readout to achieve low-noise and high-speed simultaneously. A prototype chip with 10×10 effective pixels is fabricated in 0.18-µm CMOS image sensor technology, and auto-correlation functions are successfully obtained from the measured data for 50kS/s.

1. Introduction

Fluorescence correlation spectroscopy (FCS) microscopy[1] is an effective tool to analyze the behavior of biological molecules labeled by fluorescent probes in a cell[2]. As shown in Fig. 1, FCS observes temporal fluctuation in the number of molecules, that is, fluorescence intensity, in a confocal volume, from which auto-correlation function (ACF) is calculated. By fitting it with a mathematical model, the number and the size of molecules can be quantitatively estimated. Multi-point FCS gives more information on intra- and inter-cell molecular transport with a cross-correlation function. The conventional FCS is based on single-photon detection, typically with a time-stamped single photon detection by an avalanche photodiode operating in the Geiger mode. For multi-point measurements, CMOS image sensors with integrated single-photon avalanche diodes (SPADs) have been studied[3]. However, SPAD-based image sensors suffer from pile-up.

In this paper, a dedicated CMOS image sensor architecture based on the pinned photodiode for the multi-point FCS is presented. To achieve a high-speed (≳1MS/s) continuous data acquisition and low-noise performance, complete pixel-parallel and multi-channel pipelined pixel structure is proposed.

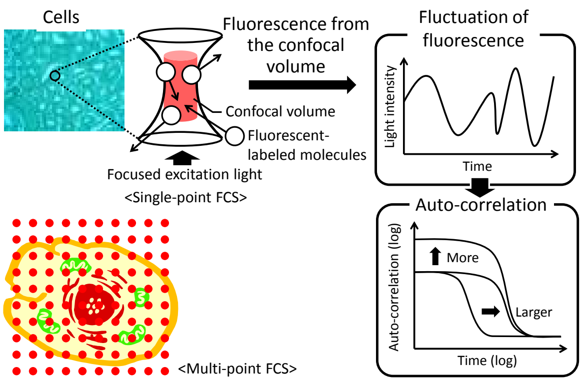

Fig. 1 Single- and multi-point fluorescence correlation microscopy.

2. Architecture

Fig. 2 shows the architecture of the proposed multi-point FCS image sensor. To achieve continuous high-speed operation, every pixel has K (=3 in the figure)

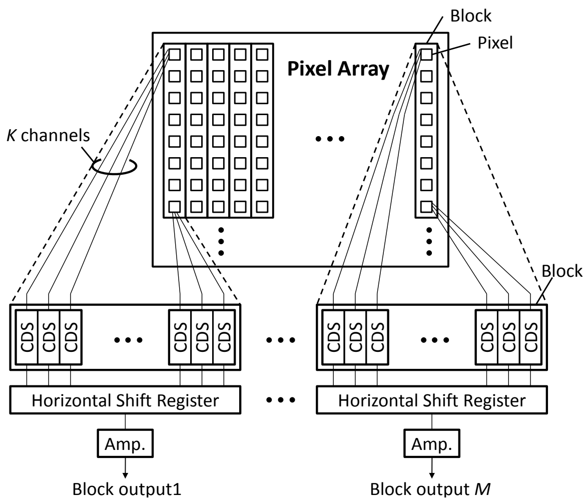

Fig. 2 Multi-point FCS image sensor architecture.

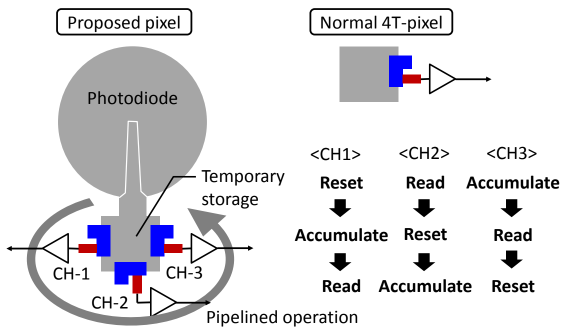

Fig. 3. Multi-channel pipelined pixel structure.

independent readout paths and the corresponding K correlated double sampling (CDS) circuits. The CDS circuits have a large gain to reduce the read noise, and are composed of 2-staged amplifiers to cancel the reset noise of the first stage. After amplification, the outputs from the pixels in the same column are sequentially read out, which contributes to significant reduction in the number of the output pin-outs to M. The pixel is based on the 4-transisntor pixel structure with a pinned photodiode, which is crucial for low noise and is free from pile-up. The photocarriers generated in the photodiode is promptly transferred to the temporary storage under a fringing electric field. Then, they are transferred to one of the K floating diffusion nodes. Figs. 3 and 4 show the pixel structure and the simplified schematic diagram and the timing chart of the read circuit. As shown in Fig. 3, the pixel operation is divided into three stages, and every channel woks simultaneously in a different stage. Thus, the speed of the amplifiers is relaxed with a factor of $1/K$, which means the noise bandwidth is narrower than that for the single-channel readout counterpart. As shown in Fig. 4, two sample-hold capacitors are prepared for each read channel, so that off-chip readout and the CDS operation can be achieved concurrently in the reset period.

3. Experimental results

The specifications and the measured characteristics of a prototype image sensor are summarized in Table I. 12-b 1-V_{pp} ADCs were followed by the image sensor. Then, the digital data were stored in a PC through digital interface. The RMS noise and the conversion gain were given by the output-referred ones, namely, they were measured at the input of the ADCs. 1LSB was about 250μV. As preliminary experiments, performances were tested for each channel. One channel was operated at 202kS/s, which was limited by the digital interface. The prototype image sensor was integrated in a microscope with an objective lens (ZEISS, C-Apo, ×40, NA/1.2, Corr). A 532-nm laser diode was used as an excitation light source. A solution with a fluorescent ink diluted with aqua pura was measured at 50kS/s in 20s. Fig. 5 compares the calculated ACFs for different pixel positions where 16-point binning, FFT, and IFFT were performed. Because the light spot was larger than one pixel in this configuration, a finite ACF was measured from the pixel next to the pixel of interest. However, for the pixels farther than one pixel, the ACFs were almost zero, which suggested that the fluctuation in the fluorescence intensity was successfully obtained.

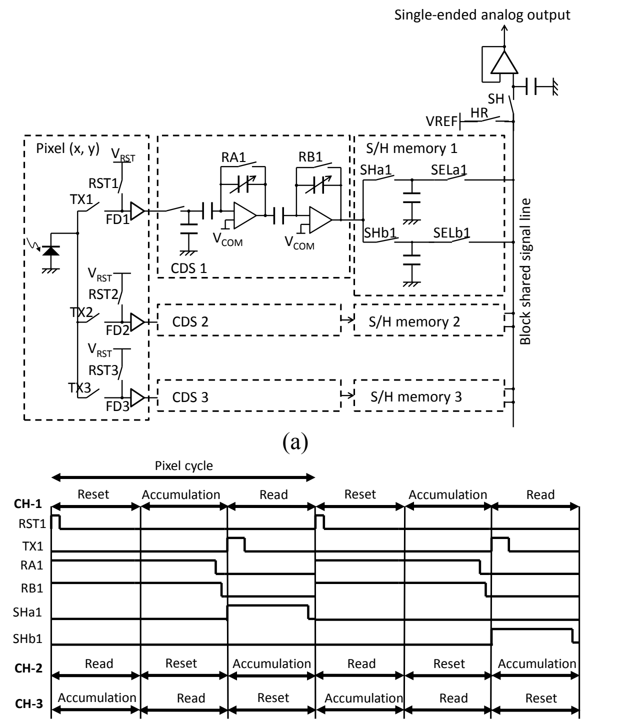

Fig. 4 (a) Simplified schematic diagram of pixel readout circuit and (b) timing chart.

4. Conclusions

A continuous high-speed CMOS image sensor based on complete parallel and multi-channel pipelined pixel readout for multi-point fluorescence correlation spectroscopy has been proposed. Auto-correlation functions were successfully retrieved with a prototype image sensor fabricated in 0.18-μm CMOS technology

Acknowledgements

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References

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Table I Specifications and measured results.

Technology	0.18-μm 1-poly 4-metal CMOS image sensor process
Pixel count	10×10 (effective area)
Pixel pitch	56 μm
Photodiode size	φ10μm
Chip size	5.0 mm sq.
Power supply	1.8 V (digital)/ 3.3 V (analog)
Pixel sampling rate	1 MS/s (maximum)
Number of analog outputs	16
CDS gain	117
RMS noise	56.6LSB @202kS/s, 1-ch
Conversion gain	14.7LSB/e-

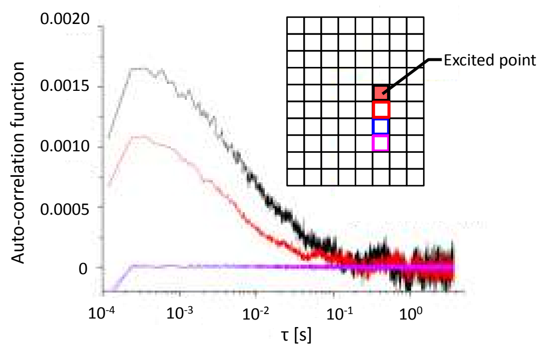

Fig. 5 Auto-correlation functions calculated from the measured data.