A Low Power Low Phase Noise PLL Quadrature Frequency Synthesizer with Optional Fast Lock-in Mode for 2.4GHz Applications

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Abstract

A low power low phase noise PLL quadrature frequency synthesizer is presented. Current reusing technique is applied to reduce power consumption and Tri-well NMOS transistors are used for VCO to improve phase noise performance. A presetting module is added to greatly shorten the PLL lock-in time. The synthesizer is implemented in 0.18\(\mu\)m CMOS process. The die area is 1.49mm\(^2\). Measured results show that the frequency tuning range is 2.16~2.55GHz. The phase noise is -124.18dBc/Hz@1MHz from 2.4GHz carrier. The power consumption is 4.98mW and the lock-in time in presetting mode is about 4\(\mu\)s.

1. Introduction

The frequency synthesizer is a key building block in wireless transceivers. It is used to obtain a pure local oscillator signal for frequency conversion in the transmitter and receiver. The design of a frequency synthesizer always needs to solve the problem of the tradeoff between the power consumption, the phase noise performance, the lock-in time and the chip die area [1].

In this paper, a low power low phase noise PLL frequency synthesizer is proposed. Great efforts were made to effectively reduce the power consumption and improve the phase noise, especially to greatly shorten the lock-in time of the PLL while maintaining a small chip area.

2. Synthesizer Architecture

Fig.1 shows the architecture of the proposed PLL frequency synthesizer. It consists of the following parts: the current reusing LC-VCO with stacked modules of a dual mode prescaler (DMP), a buffer (BUF) and a divide-by-2 circuit (DIV-2); the frequency presetting module [2]; the phase frequency detector (PFD); the charge pump (CP); the third-order low pass filter (LPF); the digital processor and the auxiliary non-volatile memory module (NVM) [3].

The PLL has two loops: the ordinary loop (O-Loop) and the fast lock-in loop (F-Loop). The lock-in time would be longer but the power consumption would be less when in O-Loop. On the contrary, the lock-in time would be significantly reduced when in F-Loop.

VCO oscillates at twice of the output frequency, and DIV-2 is used to generate quadrature I/Q signals with minimal mismatch. The current reusing technique is adopted to reduce power consumption: VCO is designed to be stacked with DIV-2, buffer and DMP. The circuit parameters of the stacked modules are optimized to meet the following relation: \(I_{LC-VCO} = I_L + I_{BUF} + I_{DMP}\).

3. Current Reusing LC-VCO

The current reusing LC-VCO with stacked modules is depicted in Fig.2. The VCO core adopts cross-coupled pair NMOS to generate negative resistance because of its lower parasitic capacitance; moreover, it can provide sufficient voltage headroom for the stacked modules. A 4-bit binary-weighted switched capacitor array is used to broaden the frequency range and lower the VCO gain [4].

M1 and M2 are Tri-well NMOS transistors and their bodies are separated from the substrate. We connect the transistor’s body to its source to avoid body effect so that the oscillation amplitude is increased and the phase noise is improved. The low supply voltage buffer not only reduces the load capacitance of DIV-2 so that the I/Q output signal amplitude is increased, but also provides a sufficient signal amplitude for DMP to enhance circuit operation stability.

4. Frequency Presetting Module

The presetting module and LC-VCO circuit are shown in Fig.3. VA is the input voltage of the presetting module. The module is a mixed-signal circuit that consists of six parallel current sources. A 6-bit digital presetting signal C<5:0> controls on and off of the current sources. The generated voltage Vctrl is the true control voltage for VCO.

The PLL has two operation modes in F-Loop: (1) the calibration mode: the relation between the output frequency...
and the presetting digital signals $C<5:0>$ and $P<3:0>$ is measured and calibrated; (2) the fast lock-in mode: the digital processor outputs the presetting signals $C<5:0>$ and $P<3:0>$ to directly preset the frequency of the LC-VCO with very small initial frequency error, as a result, the PLL can be locked within a very short time.

Fig.3 LC-VCO with presetting module

5. Auxiliary Non-Volatile Memory

The architecture of the proposed NVM is depicted in Fig.4. It is based on FN tunneling phenomenon with extremely small current density [3]. The frequency presetting signals $C$ and $P$ are stored in it after calibration. The bit-line controller controls the writing operation of the NV memory. The column decoder selects the active column. The sense amplifiers detect the outputs of the active-column cells in reading operation. The charge pump generates high voltage and MV in writing operation.

Fig.4 Architecture of the propose NVM

6. Measurement Results

The proposed PLL is implemented in 0.18μm CMOS process. The chip die microphotograph is shown in Fig.5. The chip core area is $1.6 \times 0.93$mm$^2$. The output frequency tuning range is from 2.16GHz to 2.55GHz.

Fig.5 Chip die microphotograph

The measured phase noise is -124.18dBc/Hz and -144.92dBc/Hz at 1MHz and 10MHz offset respectively from 2.4GHz carrier, shown in Fig.6. The typical lock-in time of F-Loop is about 4μs, depicted in Fig.7. The measured power consumption is 6.42mW and 4.98mW for O-Loop and F-Loop respectively. The reference frequency in this design is 1.25MHz. The synthesizer performance is summarized in Table I.

Fig.6 Measured phase noise from 2.4GHz carrier

Table I Comparison of synthesizer performance

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<tr>
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<td>Process</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
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<tr>
<td>Die Area</td>
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<td>2.1 mm$^2$</td>
<td>1.49mm$^2$</td>
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<td>Power(mW)</td>
<td>3.5</td>
<td>14.1</td>
<td>4.98/6.42</td>
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<tr>
<td>Freq. Range</td>
<td>2.4~2.48GHz</td>
<td>2.4~2.48GHz</td>
<td>2.16~2.55GHz</td>
</tr>
<tr>
<td>Lock-in Time</td>
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<td>-</td>
<td>90us/4us</td>
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<td>Phase Noise @1MHz</td>
<td>-112dBc/Hz</td>
<td>-121dBc/Hz</td>
<td>-124.18dBc/Hz</td>
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<td>@3MHz</td>
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<td>@1MHz</td>
<td>2.45GHz carrier</td>
<td>2.44GHz carrier</td>
<td>2.4GHz carrier</td>
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</table>

7. Conclusions

A low power low phase noise frequency synthesizer was presented in this paper. The synthesizer has a presetting module which greatly reduces the lock-in time. Measured results show that it has an outstanding performance.

Acknowledgements

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References