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Envelope Tracking CMOS Power Amplifier with High-speed CMOS Envelope Amplifier for Mobile Handsets

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1. Abstract

This paper presents a high-efficiency CMOS power amplifier (PA) based on envelope tracking (ET) technique for WCDMA and LTE application. By adopting a high-speed CMOS envelope amplifier (EA) with current direction sensing, 5% improvement in total power-added efficiency (PAE) and 11 dB decrease in adjacent channel leakage ratio (ACLR) are achieved with a W-CDMA signal. Moreover, the proposed PA achieves PAE of 25.4 % for a 10 MHz LTE signal at output power (Pout) of 25.6 dBm and a gain of 24 dB.

2. Introduction

A fully integrated PA in CMOS process is one of the biggest challenges to realize an ideal RF system-on-a-chip (SOC) which includes both RF and extensive digital processing. The main challenge to realize a CMOS PA is to improve the efficiency which is currently lower than that of conventional PAs based on III-V compound semiconductor.

Signals in recent wireless standards such as W-CDMA and LTE, which can communicate with higher data rate, exhibit higher peak to average ratio (PAPR) and wider channel band width. This requires high linearity for PAs in order to meet signal quality specification at the transmitting antenna. Conventional linear PAs can satisfy the linearity requirement by operating at a large back-off region. This leads to lower efficiency because PAs operate at a lower level than their saturated output power which shows maximum efficiency.

Recently, an envelope tracking PA (ET-PA), which can operate at saturated power region by changing the drain voltage according to the envelope of modulated RF signal, has been reported to achieve high efficiency [1][3]. Although several ET-PA based on III-V compound semiconductor have been reported, there haven't been CMOS ET-PA complying with the 3GPP-LTE standards yet. In this paper, we present for the first time CMOS ET-PA for W-CDMA and LTE application to achieve higher efficiency.

3. CMOS Envelope Tracking PA Design

Figure 1 shows a block diagram of ET-PA system evaluated in this paper. The PA is a fully–integrated triple-band linear CMOS PA utilizing high break-down voltage transistor, which covers a frequency range of 0.8, 1.7 and 2.0 GHz [2]. Since the internal circuit in this PA operates differentially by using center-tapped input and output transformers, less capacitance is achieved to stabilize power supply (Vdd) and this enable EA to change Vdd with high speed and high accuracy.

The basic topology of the CMOS envelope amplifier is based on a hybrid switching amplifier (HSA) combining a class-AB buffered linear amplifier and a switching mode buck converter as shown in figure 2. The linear stage provides the high-frequency current to keep linearity through the voltage feedback and the switching stage supplies the most of current with high efficiency. Conventionally, the switching stage operates as to decrease the linear stage current by comparing the measurement current flowing out of the linear stage with the given threshold level. This requires a current sensor and a comparator, resulting in the complex circuit and generating the switching delay causing the low efficiency [3]. Since the proposed HSA operates by detecting only the direction of the output current using the replica of output stage, the simple and less delayed switching circuit is achieved.

Both PA and HSA were fabricated in a 90-nm CMOS process and figure 6 shows the photograph of HSA before mounting to the evaluation board. The bandwidth of the designed HSA is about 40 MHz and the power efficiency is 80% at PA Pout of 28.5 dBm for a WCDMA signal.

4. Measurement Results

Figure 3 shows a 1.95GHz Continuous Wave (CW) measurement result where Vdd varies from 3.6 to 0.8 V. The maximum PAE of the PA is 41% at the output power of 31dBm. Since the gain of CMOS PA has the large dependence on Vdd, the envelope modulation is required to keep the gain constant over wide output power range in order to avoid the amplitude distortion. The envelope modulation function, which is easily installed in the recent transceiver, is emulated with the signal generator in this paper. By adopting ET with envelope modulation, ACLR of 11dB are improved compared with the constant Vdd of 3.4V at the average Pout of 28.5dBm for a W-CDMA signal as shown in figure 4. The ET technique improves not only PAE but also ACLR due to the constant gain at a higher output power range.

Figure 5 shows the measured gain, ACLR, and PAE versus Pout for a 10MHz LTE signal with PAPR of 7dB. PAE of 25.4% at Pout of 25.6dBm and a gain of 24dB are achieved at ACLR_E-UTRA of -32.3 dBc and ACLR_UTRA of -34.8 dBc. Figure 6 shows a summary of our ET-PA and state-of-the-art CMOS PAs.

5. Conclusions

We presented a high-efficiency CMOS ET-PA complying with W-CDMA and 10MHz LTE, focusing on the efficiency and distortion. The high-speed CMOS EA with current direction sensor enabled CMOS PA to achieve PAE of 25.4% for a 10MHz LTE signal. We believe that ET-PA in CMOS is the promising technology to realize an ideal RF SOC for small and low cost mobile handsets.

References

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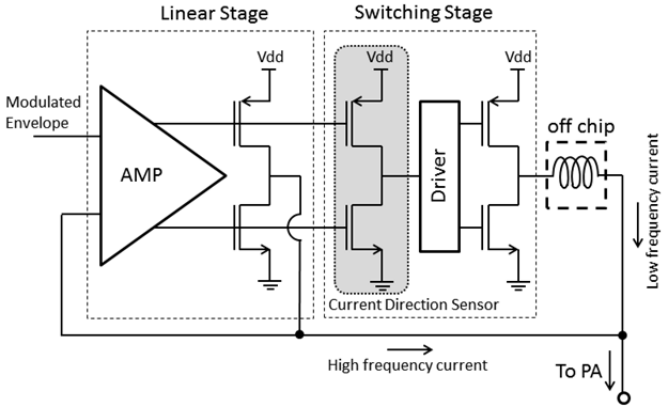

Fig. 2 Schematic of designed CMOS envelope amplifier.

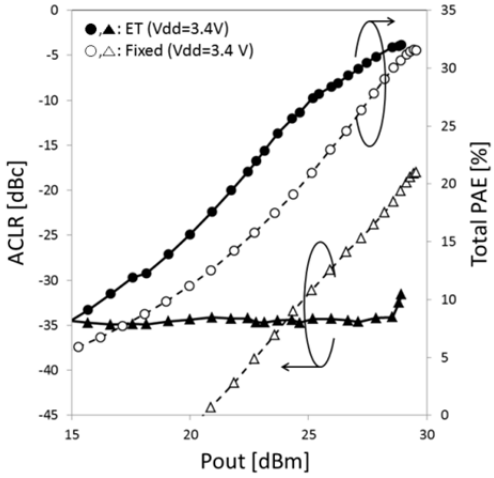

Fig. 4. Comparison of PAE and ACLR in the case where the ET or fixed Vdd is adopted for a W-CDMA signal.

Table. 1. Performance comparison of state of the art CMOS PAs

	This Work		[2]	[4]	[5]
Standard	WCDMA	LTE10M	WCDMA	LTE20M	LTE10M
Ferq [GHz]	1.95	1.95	1.95	1.8	0.93
Pout [dBm]	28.5 (ACLR <-34dBc)	25.6 (ACLR_E-UTRA <-32dBc)	27.4 (ACLR <-34dBc)	21.3 (EVM <-22dB)	26 (EVM <-22dB)
PAE [%]	31.8	25.4	28.5	18	17
Technology	90nm	90nm	90nm	65nm	90nm

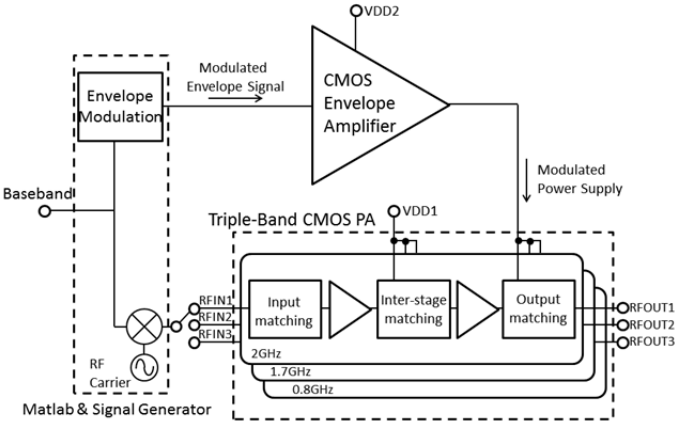

Fig. 1. Block diagram of the envelope tracking power amplifier performance measurement system.

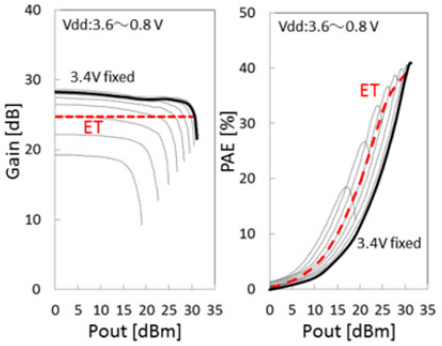

Fig. 3.Measured 1.95GHz CW characteristics. The dotted line shows Gain and PAE when ET with envelope modulation is adopted.

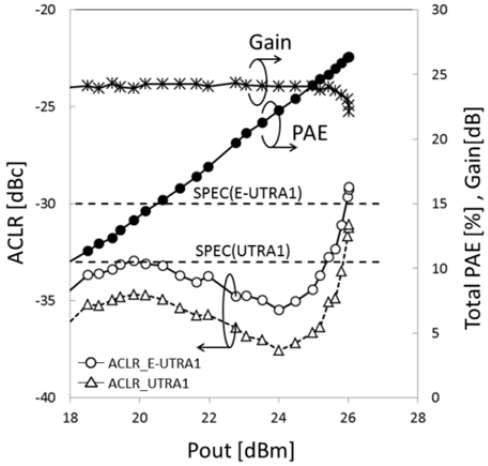

Fig. 5. Measurement results of PAE, Gain and ACLR versus Pout for 10 MHz LTE signal at 1.95 GHz.

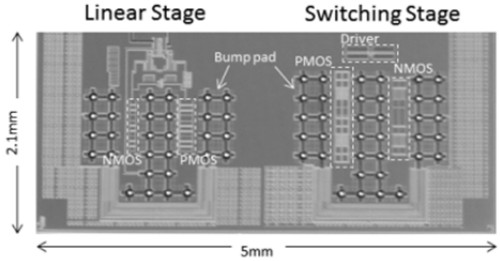

Fig. 6. Fabricated chip photograph of CMOS EA.