Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp914-915

Au-Free Low Temperature Ohmic Contacts for AlGaN/GaN Power Devices on 200 mm Si Substrates

A. Firrincieli, B. De Jaeger, S. You, D. Wellekens, M. Van Hove and S. Decoutere
imec
Kapeldreef 75, B-3001 Leuven, Belgium
Phone : +32 16 287790 E-mail: firrin@imec.be

Abstract

We report on the fabrication and characterization of Au-free Ti/Al/TiN-based ohmic contacts on AlGaN/GaN epilayers for power devices. Materials and processing used are fully compatible for integration of GaN-based devices in a Si platform. Contact resistance values as low as 0.62 Ω·mm were measured for an optimum alloy temperature as low as 550 °C.

1. Introduction

GaN-based high electron mobility transistor (HEMT) technology offers perspectives for power device performance beyond the Si limitations. However, such devices are today fabricated on small diameter wafers, and often on SiC substrates. To reduce fabrication costs, GaN HEMT power devices should be fabricated on standard large diameter Si substrates in high-productivity CMOS production facilities.

GaN HEMT device integration in a Si CMOS platform requires, besides other challenges, the implementation of Au-free metallization schemes for source/drain ohmic contacts. A typical metallization scheme consists of the deposition of a metal stack directly on top of the AlGaN layer, followed by a rapid thermal annealing (RTA) step at a sufficiently high temperature to form a metal/AlGaN alloy. In addition, prior to the metal stack deposition, one or several treatments (wet clean, exposure to a plasma, recess etching ...) can be applied to the AlGaN/GaN HEMT epilayer. Typically the most successful metallization schemes have been using Au-containing metal stacks annealed at relatively high temperatures (≥ 800 °C), achieving typical contact resistance (R_C) values below 1 Ω·mm.

In recent years, several Au-free contact schemes have been proposed, aiming at similarly low R_C. The most frequently cited metallization schemes are Ti/Al-based, such as Ti/Al/W [1] and Ti/Al/Ni/Ta/Cu/Ta [2]. In these cases, R_C below 1.0 Ω·mm has only been demonstrated at relatively high annealing temperatures (≥ 800 °C). Low R_C and low annealing temperature for Au-free schemes have also been published, but typically used metal schemes not directly compatible with CMOS platforms. For example, using a Ta/Al metal stack, a R_C value of 0.06 Ω·mm has been reported [3]. Low R_C values were also obtained with the introduction of Si doping in the GaN and/or AlGaN layer. This, however, can cause problems for the breakdown voltage of power devices, and Si implantations in GaN-based layers typically require annealing at very high temperatures (>1000 °C), not compatible with the process flow.

In this work we report on the fabrication of ohmic contacts for AlGaN/GaN power devices using a Ti/Al/TiN-based metal stack. We optimized the thickness of the initial Ti/Al bottom layers and obtained a contact resistance of 0.62 Ω·mm with an alloy temperature as low as 550 °C.

2. Experiment Details

Undoped AlGaN/GaN/AlGaN double heterostructure layers grown on 200 mm Si by MOCVD are used. On the Si substrate a 200 nm-thick AlN nucleation layer is first grown, followed by a buffer layer consisting of 400 nm $Al_{0.75}Ga_{0.25}N$, 400 nm $Al_{0.44}Ga_{0.56}N$, and 1800 nm $Al_{0.2}Ga_{0.8}N$. Next the 150 nm-thick GaN channel is grown followed by a thin AlN spacer and by a 15 nm $Al_{0.2}Ga_{0.8}N$ barrier layer. Finally, a 2 nm GaN layer is used as capping layer.

A 150 nm-thick *ex situ* SiN passivation layer is deposited by rapid thermal chemical vapor deposition (RTCVD) at 700 ºC. This layer is fundamental to adequately passivate the 2-dimensional electron gas (2DEG) that forms at the AlGaN/GaN interface and to avoid surface depletion.

The formation of ohmic contacts starts with a dry etch step of the RTCVD nitride and the AlGaN barrier in the contact area down to the location of the 2DEG in the GaN channel (Fig. 1). A HCl-based clean is then carried out prior to the metal deposition. Rapid Thermal Annealing (RTA) at 550 °C in N_2 ambient for 90 s completes the formation of the ohmic contact.

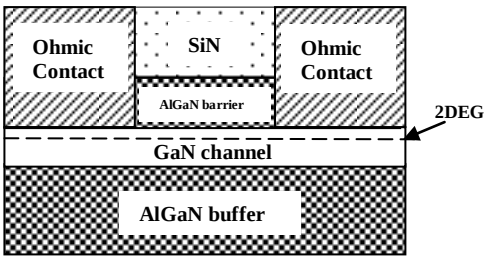

Fig. 1 Schematic of recessed ohmic contacts to a AlGaN/GaN HEMT.

The CMOS-compatible metal stack used for ohmic contacts is a Ti/Al/TiN-based stack with a fixed thickness of 60 nm for the TiN cap. The importance of the Ti/Al thickness ratio has already been studied [4, 5], explaining the role of Al in reducing the aggressive Ti-GaN reaction,

while excess of Ti would lead to the formation of voids below TiN [5, 6]. Saturation of current through ohmic contacts to AlGaN/GaN HEMT layers has been investigated and different theories have been proposed as explanation such as the self-heating causing velocity saturation [7] or the impact of surface traps acting as a 'virtual gate' depleting locally the 2DEG [8].

Ohmic contacts are characterized with the standard transfer length method (TLM) [9]. Together with the extraction of R_C and the sheet resistance of the 2DEG, we measured the current at 10 V through 12 µm-spaced ohmic contacts. Moreover, we investigated the correlation of R_C with the maximum current through the ohmic contacts.

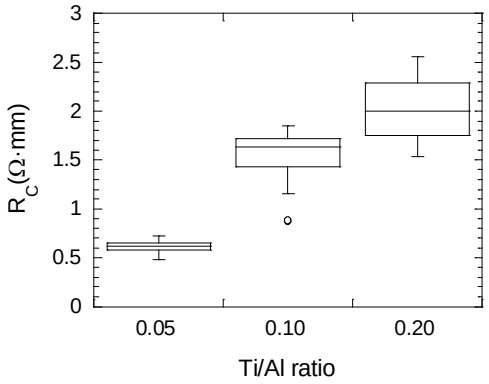

Fig. 2 Extracted R_C values versus the Ti/Al ratio.

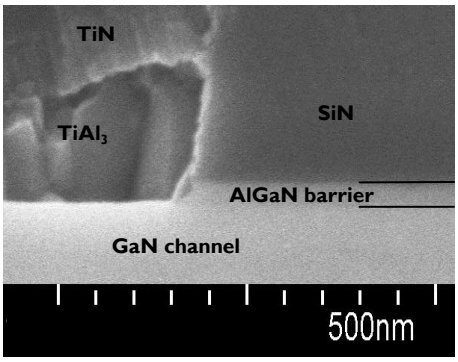

Fig. 3 Cross-section SEM image of optimized ohmic contacts.

3. Results and Discussions

The 2DEG sheet resistance at the AlGaN/GaN interface was extracted on Van der Pauw structures and the value obtained is 400 ± 10 Ω/sq over the full 200 mm wafer, assessing a good quality and uniformity of the 2DEG. The box chart shown in Fig. 2 shows the median value and the spread over the 200 mm wafer for the R_C values obtained when changing the Ti/Al ratio in the ohmic metal stack. It was found that optimization of the Ti/Al ratio results in lower R_C, together with a smaller spread over the 200 mm wafer, with a minimum value of 0.62 ± 0.06 Ω·mm obtained for a Ti/Al ratio of 0.05. Fig. 3 shows a cross-section scanning electron microscopy image of the recessed ohmic contact after alloy at 550 °C, forming $TiAl_3$, together with the unreacted TiN cap. A smooth and sharp interface is observed between the metal contact and the GaN channel surface. In Fig. 4 the I-V wafer mapping over the full 200 mm wafer up to 10 V for two wafers with different Ti/Al ratio is compared. The wafer with 0.05 Ti/Al ratio with lowest R_C is also showing a higher current at 10 V (~0.6 A/mm).

We have previously reported on Au-free ohmic contacts with low R_C using a Ti/Al/W metal stack alloyed at 600 ºC [10]. The present study however allows to further lower the thermal budget to 550 °C and the TiN metal cap is commonly used in Ti/Al-based CMOS interconnects.

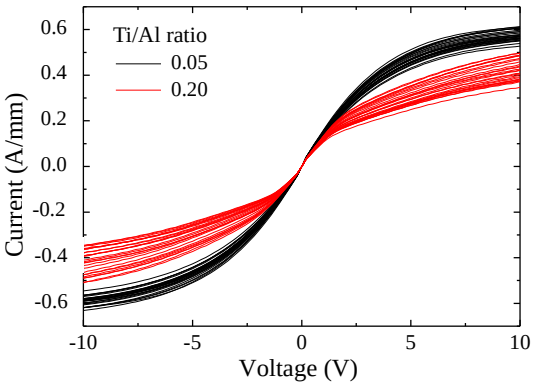

Fig. 4 I-V characteristics up to 10 V for contacts with low and high R_C. The contact spacing is 12 µm.

4. Conclusions

In this work we fabricated ohmic contacts for AlGaN/GaN HEMTs on 200 mm Si substrates in a fully CMOS-compatible integration scheme. With a standard Ti/Al/TiN-based metallization scheme an optimal R_C value of 0.62 Ω·mm was obtained for a Ti/Al ratio of 0.05 and an annealing temperature as low as 550 °C. The current through the ohmic contacts at 10 V was 0.6 A/mm, showing a correlation between low R_C and high saturation current. Our results are encouraging in demonstrating the possibility to integrate high quality AlGaN/GaN HEMTs on standard Si CMOS platforms.

References

[1] H. S. Lee *et al.*, IEEE Electron Device Lett. **32** (2011) 623.

[2] M. Alomari *et al.*, ECS Trans. **25** (2009) 33.

[3] A. Malmros *et al.*, Semicond. Sci. Technol. **26** (2011) 075006.

[4] B. Jacobs *et al.*, Journal of Crystal Growth **241** (2002) 15.

[5] X. Kong *et al.*, J. Phys. D **45** (2012) 265101.

[6] B. Van Daele *et al.*, Appl. Phys. Lett. **87** (2005) 061905.

[7] S. A. Vitusevich *et al.,* Appl. Phys. Lett. **82** (2003) 748.

[8] J. Kuzmik *et al.*, J. Appl. Phys. **99** (2006) 123720.

[9] D. K. Schroder "*Semiconductor Materials and Device Characterization*", Wiley, New York (1998).

[10] M. Van Hove *et al.*, IEEE Electron Device Lett. **33** (2012) 667.