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Impact of PdO Gate Interlayer on the DC Performance of GaN/AlGaN High Electron Mobility Transistor

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Abstract

We demonstrate significant improvements of GaN/AlGaN high-electron- mobility-transistor (HEMT) by employing PdO gate interlayer which exhibit device performance superior to that of Pd Schottky gate HEMTs. The PdO gate interlayer effectively reduces the gate leakage current by four orders of magnitude and it also increases the I_{ON}/I_{OFF} ratio to four orders of magnitude. The improved AlGaN/GaN/PdO HEMT shows a nearly ideal sub-threshold slope of 66 mV/dec. A lower flicker noise characteristic is also observed in the PdO-Gate HEMTs compared with Pd-Gate HEMT. The high work function PdO layer and associated barrier height enhancement is believed to be the origin of improved device performance.

1. Introduction

GaN/AlGaN high-electron-mobiliy-transistor (HEMT) is widely studied for high power and high frequency applications. Conventional Schottky gate limits the device performance owing to large gate leakage current. Consequently several approaches have been proposed to reduce gate leakage current and a variety of gate oxide in MOS gate structures has been reported. However, by inserting a oxide layer between the gate metal and Schottky barrier layer leads to shift of threshold voltage owing to series impedance of the oxide material and interface/fixed oxide charge.The high work function conducting metal oxide could be another possible way of enhancing Schottky barrier height to reduce gate leakage and improve device performance. Palladium oxide (PdO) is a material with high thermal and chemical stability. Its work function can reach up to 7.9 eV depending on the surface orientation and termination. [1] In this study, we fabricated AlGaN/GaN HEMTs with PdO gate interlayer and compared device characteristics with those of Pd Schottky gate devices.

2. Experimental Procedure

The epitaxial structure of GaN/AlGaN heterostructure was grown by MOCVD system on P-type silicon substrate. Hall measurement revealed a 2-DEG density of ~1.122×10^{13} cm^{-2} and electron mobility of 1170 $cm^2V^{-1}s^{-1}$. Device isolation was performed by mesa dry etching in a BCl_3 plasma RIE chamber. Ohmic contacts comprised of Ti/Al/Ni/Au metals were deposited through electron beam (EB) evaporation, followed by RTA process at 850°C for 30 s in a N_2 ambient. A 10 nm Pd was evaporated at an O_2 flow rate of 20 sccm. Then Pd/Au (70/140 nm) gate metals were deposited. For comparison, a Pd/Au Schottky gate AlGaN/GaN HEMT was also fabricated with similar process flow except the PdO layer formation. The gate dimensions for both devices are 1×100 μm^2 with a source to drain spacing of 6 µm. Finally, 200 nm SiO_2 was deposited for device passivation. A schematic cross-sectional structure of a PdO/AlGaN/GaN HEMT is presented in Fig. 1.

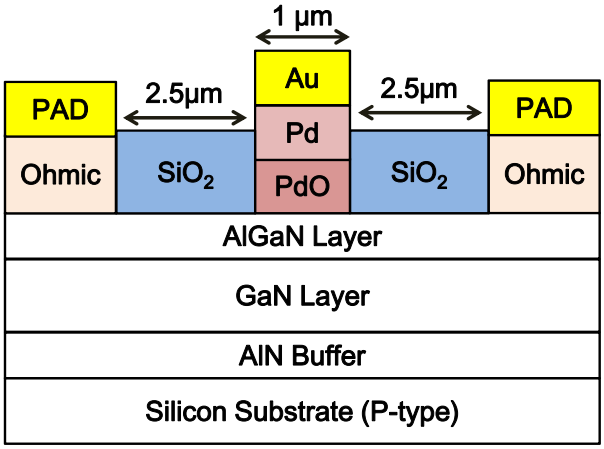

Fig. 1 Schematic illustration of fabricated GaN/AlGaN HEMTs with PdO Gate interlayer.

3. Results and Discussion

Figure 2 shows well behaved I_{DS}-V_{DS} characteristics of PdO interlayer HEMTs and Pd Schottky gate HEMTs.

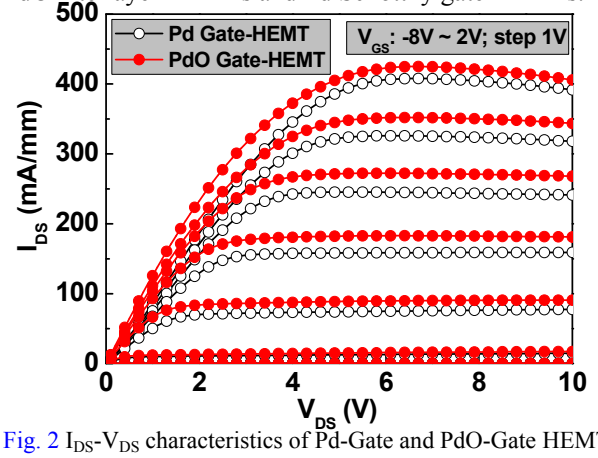

Fig. 2 I_{DS}-V_{DS} characteristics of Pd-Gate and PdO-Gate HEMT when V_g varies from -8 to 2 V at a step of 1 V.

We measure the drain current (I_{DS}) as a function of the gate-to-source voltage (V_{GS}) for both devices biased at V_{DS} = 8 V. The I_{ON}/I_{OFF} ratio and SS of the PdO-Gate HEMT (1.2×10^{9} and 66 mV/dec) are superior to those of the Pd-Gate HEMT (9.5×10^{5} and 122 mV/dec), suggesting excellent gate control of the 2DEG channel as shown in Fig. 3. Figure 3 also shows OFF-state I_{DS} which reveals that the leakage current of 7.1×10^{-4} mA/mm for Pd-Gate devices is decreased to 4.3×10^{-8} mA/mm, after insertion of the PdO thin layer. No apparent threshold voltage shift is observed for PdO-Gate HEMT owing to conducting nature of PdO layer.

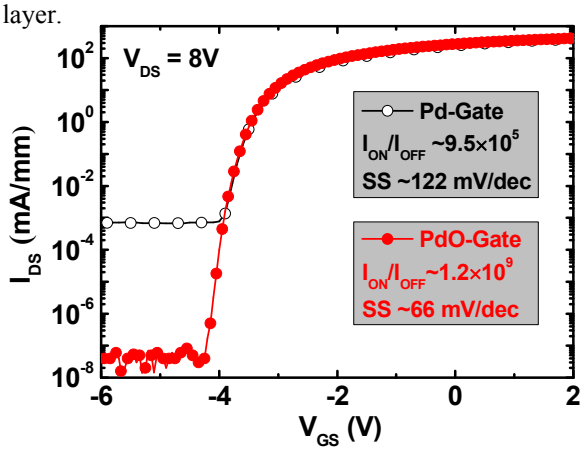

Fig. 3 Semi-log I_{DS}-V_{GS} characteristics of Pd-Gate and PdO-Gate HEMT with constant V_{DS}=8 V.

Figure 4 shows gate leakage current density of the Pd-Gate and PdO-Gate HEMTs. The leakage current density of PdO-Gate HEMT reaches as low as 8.96×10^{-8} mA/mm at V_{GD} of –10 V; this value is four orders of magnitude lower than that of the Pd-Gate HEMT (2.38×10^{-4} mA/mm). Schottky barrier height is calculated from measured I-V data. According to the respective log (I_{GD}) vs. V_{GD} showing in the Fig. 5, calculated Schottky barrier heights for the PdO-Gate and Pd-Gate HEMT are 0.884 eV and 0.716 eV respectively**.** The higher Schottky barrier height of PdO-Gate HEMT is owing to higher work function of PdO than that of Pd. [2]

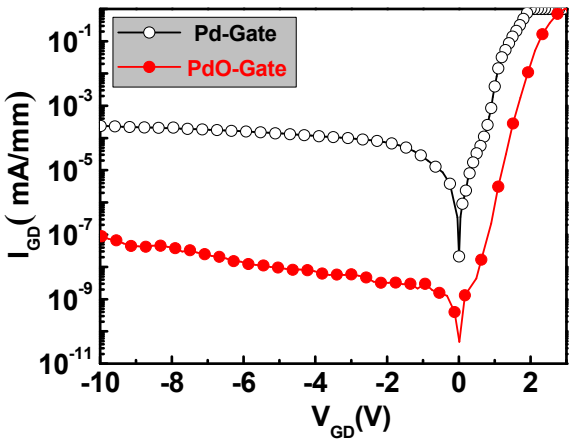

Fig. 4 Gate leakage current of the Pd-Gate and PdO-Gate HEMTs.

The flicker noise measurement is conducted to elucidate the relationship between the low frequency noise and gate electrode interface. During measurement, the frequency is varied from 1 Hz to 100 kHz and gate bias (V_{GS}-V_{th}) is varied from 0.2 to 0.8 V with +0.2 V steps. Figure 5 shows the measured frequency-dependent normalized 1/f flicker noise spectra, S_{ID}/I_D^2 of the PdO-Gate and Pd-Gate HEMTs at V_{DS}=8 V. The PdO-Gate HEMT has a lower flicker noise spectra compared to Pd-Gate HEMT, because the PdO-Gate HEMT has low gate leakage current. It indicates that lower surface states can be achieved with this reactive EB evaporated PdO film

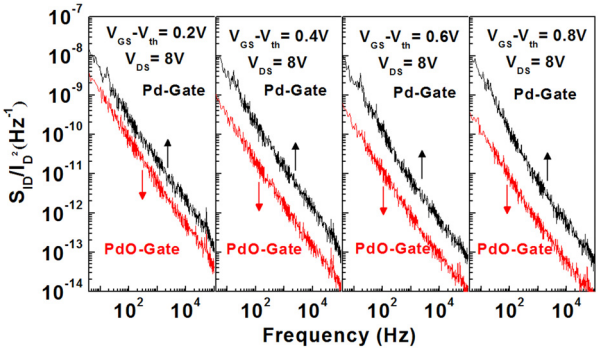

Fig. 5 Normalized of S_{ID}/I_D^2 with various (V_{GS}-V_{th}) for both PdO-Gate and Pd-Gate HEMTs.

Comparing both kinds of devices, significant improvement in the OFF state characteristics i.e. sub-threshold drain leakage current and gate leakage current for PdO-Gate HEMT are observed owing to the high work function PdO gate interlayer and associated barrier height enhancement. In addition, PdO interlayer effectively suppresses the surface states underneath the Pd Schottky gate which results lower flicker noise characteristic for PdO-Gate HEMT.

4. Conclusions

PdO layer is prepared through reactive EB evaporation under a high oxygen flow and applied it as gate interlayer in GaN/AlGaN HEMTs. The gate leakage current and OFF-state drains current are effectively reduced by high-work function PdO layer. As a result of lower leakage current and lower interface traps, a nearly ideal sub-threshold slope of 66 mV/dec and higher I_{ON}/I_{OFF} ratio are obtained in PdO-Gate HEMT devices. This high work function PdO film may render potential application in GaN/AlGaN HEMT technology for future device development.

Acknowledgements

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