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Scaling to 100nm Channel Length of Crystalline In-Ga-Zn-Oxide Thin Film Transistors with Extremely Low Off-State Current

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1. Introduction

C-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) is an oxide semiconductor which has a c-axis aligned crystal structure [1]. This material has been used as an active layer of a thin film transistor (TFT) for achieving displays with high definition and low power consumption [2]. A CAAC-IGZO TFT has an extremely low off-state current [3], and its applications have been proposed in the field of LSIs such as a nonvolatile memory, a CPU, and an image sensor [4-6]. In order to expand the versatility of the CAAC-IGZO for LSIs, device size scaling is essential. It is reported that existing IGZO TFTs have immunity to the short channel effect [7].

We report, for the first time, device characteristics of CAAC-IGZO TFTs with channel lengths scaled from 1 μm to 100 nm. The results demonstrate that the off-state current I_{OFF} is lower than the usual measurement limit (~ 1×10^{-13} A) regardless of the channel length L. They have excellent short-channel characteristics in that even when a gate insulator EOT (Equivalent Oxide Thickness) is 11 nm and L is 100 nm, DIBL is 39 mV/V and SS is 74 mV/dec. Such an extremely low I_{OFF} has not been reported in exiting short-channel IGZO TFTs [7] and Si transistors.

2. Experiments

Fig. 1 summarizes a fabrication process of the CAAC-IGZO TFT used in this work. A CAAC-IGZO active layer was deposited by DC sputtering of a target with an atomic ratio of In:Ga:Zn = 1:1:1 in an ultrapure atmosphere of Ar and O_2. The CAAC-IGZO TFT has the device structure whose gate electrode overlaps with the source/drain (S/D) electrodes. In addition, it does not need any n+ doping of the active layer to reduce the contact resistance with the S/D electrodes. The channel length L and the channel width W are defined as a distance between the S/D electrodes and a width of the CAAC-IGZO island, respectively. Fig. 2 (a) shows an X-ray diffraction spectrum of the CAAC-IGZO film formed over a quartz substrate under the above-described conditions, and shows a (009) diffraction peak attributable to the CAAC structure with a unit cell as shown in Fig. 2(b). Actually, a layered crystal structure can be clearly observed in a cross-sectional TEM image of the CAAC-IGZO film as shown in Fig. 2 (c).

3. Device characteristics

Figs. 3 and 4 show I_d-V_g characteristics and I_d-V_d characteristics, respectively, of a CAAC-IGZO TFT with W/L = 50 nm/100 nm and a gate insulator EOT=11 nm. The on-state current I_{ON} at V_g = 2.7 V and V_d = 1 V is 46 μA/μm. Remarkably, the I_{OFF} is lower than the measurement limit (~ 1×10^{-13} A) of usual semiconductor parameter analyzers at V_g= -0.3 V. Figs. 5-7 show L dependences of V_{th}, DIBL, and SS, respectively, at V_d = 1V. The TFTs have excellent short-channel characteristics even for the gate insulator EOT of 11 nm and with the gate overlapped structure. The TFT with L = 100 nm has DIBL of 39 mV/V and SS of 74 mV/dec. An IGZO TFT is an accumulation-mode TFT in which electrons serve as majority carriers, and the electric fields extending from the S/D to the channel are screened in short ranges. This results in high controllability of carrier density with a gate electric field, and thus the IGZO TFT has immunity to the short channel effect.

The I_{ON}-I_{OFF} characteristic of Fig. 8 shows that I_{OFF} of the CAAC-IGZO TFT is too low to detect by usual measuring means. We devised a method to detect a very low current [3], and measured I_{OFF} of the CAAC-IGZO TFT with a wide channel width of 10mm and a sub-μm channel length of 500 nm. The I_{off} at V_g = -3 V was estimated to be 60 yA/μm at 85 °C ("y"; yocto = 10^{-24}) as shown in Fig. 9. In order to explain the mechanism for this extremely low I_{OFF}, Fig. 10 shows an energy band diagram of an IGZO TFT in an off state. Due to negative gate bias and the wide band gap of E_g ~ 3.2 eV of the IGZO, electron and hole thermal diffusion currents do not flow. Besides, because holes have a very large effective mass of approximately 10 m_0, hole tunneling current does not flow either. In addition to such reasonings in terms of the band theory, it is important that our CAAC-IGZO film has few recombination centers in the band gap. These properties ought to be obtained basically even with L < 100 nm.

4. Conclusions

This work has demonstrated that our CAAC-IGZO TFTs have extremely low I_{OFF} even when channel lengths are scaled down to 100 nm. Moreover, they have excellent short-channel characteristics even for the gate insulator EOT of 11 nm and with the gate overlapped structure. It can be expected that further scaling of the TFTs leads to new LSI applications which cannot be realized with Si-based devices, utilizing the extremely low I_{OFF}.

References

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[3] K. Kato *et al.*, Jpn. J. Appl. Phys., **51**, 021201, 2012.
[4] H. Inoue *et al.*, IEEE JSSC, **47**, 2258, 2012.
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[6] T. Aoki *et al.*, VLSI Tech. Dig., pp. 174-175, 2011.
[7] S. Jeon *et al.*, IEDM Tech. Dig., pp. 504-507 , 2010.

● **Fabrication Process of CAAC-IGZO TFT**
- **Silicon wafer**
- **Base insulator film deposition (EOT∼390 nm)**
- **CAAC-IGZO film deposition (t_{IGZO}∼5 nm)**
- **CAAC-IGZO film patterning**
- **Source/Drain electrode formation**
- **Gate insulator film deposition (EOT∼11 nm)**
- **Gate electrode deposition**
- **Gate electrode and gate insulator film patterning**
- **Passivation formation**

Fig. 1 Fabrication process of the CAAC-IGZO TFT.

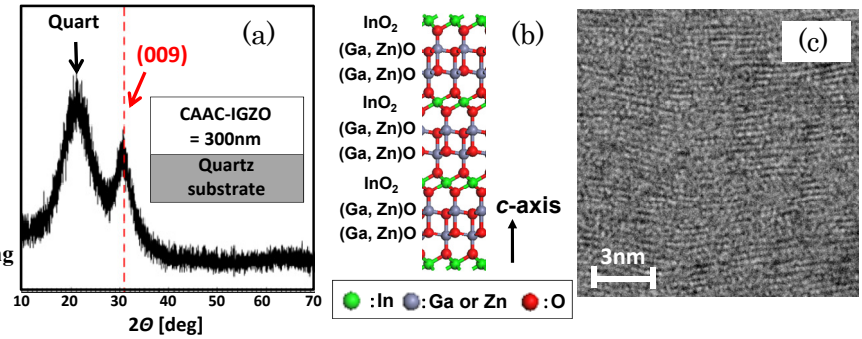


Fig. 2 (a) Out-of-plane XRD spectrum of a CAAC-IGZO. (b) Conceptual diagram of the single crystal $InGaZnO_4$ in the c-axis direction. (c) Cross-sectional STEM image of a CAAC-IGZO film.

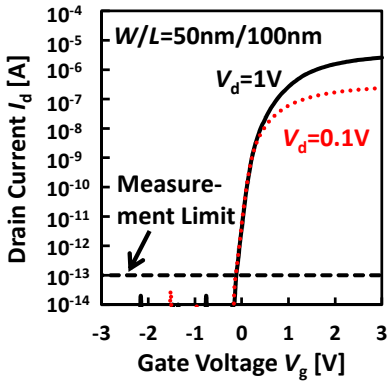


Fig. 3 I_d-V_g characteristics of a CAAC-IGZO TFT with W/L = 50 nm/100 nm.

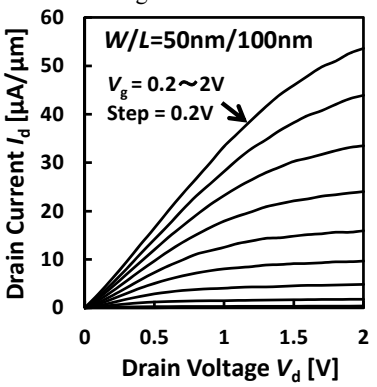


Fig. 4 I_d-V_d characteristics of a CAAC-IGZO TFT withW/L = 50 nm/100 nm.

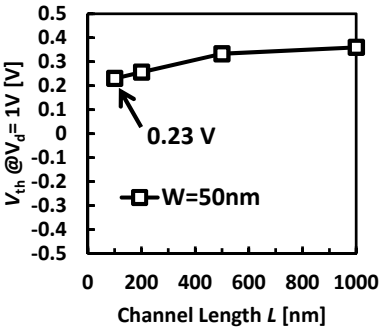


Fig. 5 Channel length L dependence of V_{th} of a CAAC-IGZO TFT. Median values for 9 devices or more are plotted.

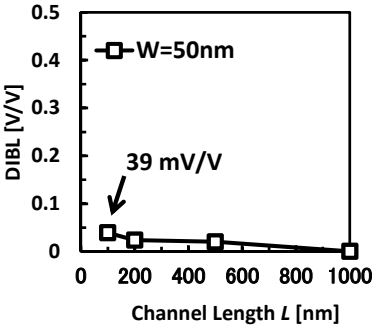


Fig. 6 Channel length L dependence of DIBL of CAAC-IGZO TFTs. Median values for 9 devices or more are plotted.

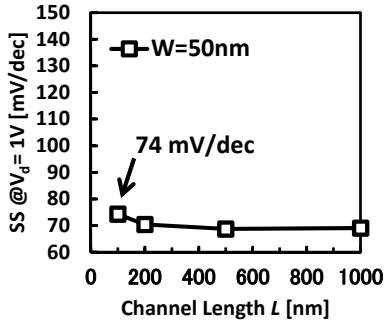


Fig. 7 Channel length L dependence of SS of CAAC-IGZO TFTs. Median values for 9 devices or more are plotted.

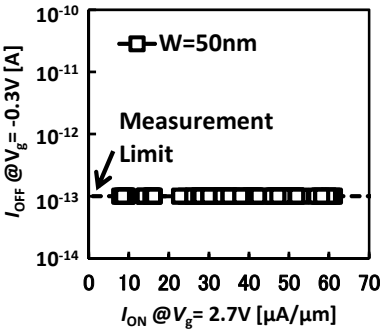


Fig. 8 I_{ON}-I_{OFF} characteristics of CAAC-IGZO TFTs. The values of I_{OFF} lower than measurement limit (∼ 1 × 10^{-13} A) in I_d-V_g characteristics are plotted at 1 × 10^{-13} A .

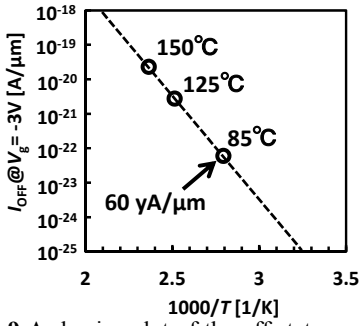
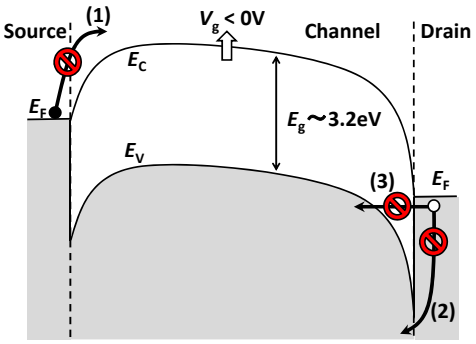


Fig. 9 Arrhenius plot of the off-state current at V_g = -3V for a CAAC-IGZO TFT with W/L = 10 mm/500 nm. The I_{off} at V_g=-3V was estimated to be 60 yA/μm at 85 °C, where the prefix "y" (yocto) is 10^{-24}.



E_C: Energy of the conduction band edge
E_V: Energy of the valence band edge
E_F: Fermi energy
E_g: Band gap

◆ **Three possible major mechanisms for an off-state current**
(1) Electron thermal diffusion
(2) Hole thermal diffusion
(3) Hole tunneling

Fig. 10 Schematic energy band diagram of an IGZO TFT in an off state.