Gate Oxide Thickness Dependence of Intrinsic Gain and Flicker Noise in InGaZnO Thin Film Transistors

T. Morooka, K. Fukase, S. Nakano*, S. Toriyama*, H. S. Momose, and T. Ohguro
Toshiba Corporation Semiconductor & Storage Products Company, *Corporate R & D center, 1, Komukai Toshiba-Cho, Saitama-Ku, Kawasaki, Kanagawa, 212-8583, Japan
Phone: +81-44-549-2801, Fax: +81-44-549-2802, E-mail: tetu.morooka@toshiba.co.jp

Abstract
Analog behavior of InGaZnO-TFTs were investigated. It was confirmed that intrinsic gain (Ran*gsn) and transconductance efficiency (gs/gm) are improved with reducing gate oxide thickness. Flicker noise also decreases in proportion to the square of thickness of gate oxide. In addition, the noise phenomena in TFTs were analyzed in detail for the TFTs with back gate electrode and two-dimensional simulations.

Introduction
Recently, amorphous oxide Thin-Film-Transistors (TFTs) have been introduced as driver TFTs in FPDs [1]. It is reported that an InGaZnO film as an active layer has great advantages of good transparency, high mobility, extremely low off current and low fabrication temperature [2,3].

In this paper, the analog behaviors of InGaZnO-TFTs are presented. The gate oxide thicknesses dependence and the gate bias dependence were investigated. In addition, the behavior of flicker noise was analyzed using the TFTs with back gate electrode and two-dimensional simulations.

Experimental
Figure 1 (a) shows the sample fabrication procedure in our experiment. After gate electrode formation, SiO2 gate dielectrics were deposited using PE-CVD. An InGaZnO film was produced by metal vapor deposition (PVD), following active area was formed. After SiO2 passivation film was deposited using PE-CVD, and annealing process was accomplished at nitrogen atmosphere. After metalization, annealing treatment was carried out again.

Figure 1 (b) shows the TEM cross-section of an InGaZnO-TFT with 12 nm gate oxide. In the structure, the channel length was determined by the distance between S/D contacts.

Results and Discussions
DC characteristics
Figure 2 shows the I-Vg curves of TFTs with 12 nm, 22 nm and 45 nm gate oxides. Good switching characteristics were obtained in 3 devices. The drain current increased with the decrease in gate oxide thickness. Figure 3 shows the threshold voltage and the subthreshold slopes of TFTs with various channel lengths. Note that in the case of 12 nm gate oxide TFTs, the excellent subthreshold slope value of about 60 mV/decade was obtained in less than 2 μm channel length devices. Although threshold voltage became lower with channel length reduction in the thicker oxide TFTs, they had good cut-off characteristics, as shown in Fig. 2.

Analog gain
Figure 4 shows the I-Vg characteristics of 2 μm channel length TFT with 12 nm gate oxide. Figure 5 shows the gate oxide thickness dependence of output resistance (Rso) and intrinsic gain (Ran*gsn). Supply voltage was 5 V. The Rso values were degraded with reducing gate oxide thickness, while the Ran*gsn values were improved. Due to their small mobility compared with that of Si MOSFETs, the Rso*gsn values themselves were not so high, but the dependency to gate oxide thickness was similar to that of Si MOSFETs.

It was also confirmed that the transconductance efficiency (gs/gm) was improved in the TFTs with thinner gate oxide at the low gate overdrive voltage (Vod/Vg) of less than 0.5 V, as shown in Fig. 6. The values of 7.5 and 7.0 were obtained in 12 nm gate oxide TFTs at Vg = 0.2 V and 1.0 V, respectively, which were comparable to those of Si MOSFETs.

Figure 7 shows the gain of an amplifier transistor in a source follower circuit. The slope, the ratio of source voltage to gate voltage (dVds/dVg), corresponds to its gain. Almost ideal unity-gain was obtained in all TFTs, because substrate bias is not applied in the structure.

Flicker noise characteristics
Figure 8 shows the frequency dependence of input-referred spectral noise density (Sv) in the TFTs with 12 nm, 22 nm and 45 nm gate oxides. Supply voltage was 5 V. It was confirmed that the Sv decreases in inverse proportion to frequency. In addition, Sv values were approximately equal in the temperature range from RT to 120°C, as shown in Fig. 9. They were extrapolated at 1 Hz, and normalized by each channel area. Figure 10 shows the gate oxide thickness dependence of normalized Sv values at RT. It was confirmed that the noise decreases in inverse proportion to thickness. The thickness even in TFTs. The results suggest that the noise in TFTs is mainly caused by carrier number fluctuation [4].

Figure 11 shows the dependence of normalized Sv values on gate overdrive voltage (Vod/Vg) in the TFTs. In the case of long channel TFTs (Lg = 10μm), the Sv values were almost the same in the wide gate bias range. In the case of short channel TFTs (Lg = 1μm), Sv values slightly degraded in the low Vod region, and improved with higher Vod bias condition.

Conclusions
The analog characteristics of InGaZnO-TFTs with gate oxides between 12 nm and 45 nm have been investigated. It was confirmed that intrinsic gain (Ran*gsn) and transconductance efficiency (gs/gm) are improved with reducing gate oxide thickness. In a source follower circuit, almost ideal unity-gain (dVds/dVg) was obtained because substrate bias is not applied in the structure. Flicker noise characteristics were also improved with gate oxide thickness reduction. It was confirmed that the noise occurs mainly by carrier number fluctuation.

References