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Gate Oxide Thickness Dependence of Intrinsic Gain and Flicker Noise in InGaZnO Thin Film Transistors

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Abstract

Analog behaviors of InGaZnO-TFTs were investigated. It was confirmed that intrinsic gain (R_{out}*g_m) and transconductance efficiency (g_m/I_d) are improved with reducing gate oxide thickness. Flicker noise also decreases in proportion to the square of thickness of gate oxide. In addition, the noise phenomena in TFTs were analyzed in detail using the TFTs with back gate electrode and two-dimensional simulations.

Introduction

Recently, amorphous oxide Thin-Film-Transistors (TFTs) have been introduced as driver TFTs in FPDs [1]. It is reported that an InGaZnO film as an active layer has the great advantages of good transparency, high mobility, extremely low off current and low fabrication temperature [2-3].

In this paper, the analog behaviors of InGaZnO-TFTs are presented. The gate oxide thicknesses dependence and the gate bias dependence were investigated. In addition, the behavior of flicker noise was analyzed using the TFTs with back gate electrode and two-dimensional simulations.

Experimental

Figure 1 (a) shows the sample fabrication procedure in our experiment. After gate electrode formation, SiO_2 gate dielectrics were deposited using PE-CVD. An InGaZnO film was produced by physical vapor deposition (PVD), following active area was formed. After SiO_2 passivation film was deposited using PE-CVD, and annealing process was accomplished at nitrogen atmosphere. After metallization, annealing treatment was carried out again.

Figure 1 (b) shows the TEM cross-section of an InGaZnO-TFT with 12 nm gate oxide. In the structure, the channel length was determined by the distance between S/D contacts.

Results and Discussions

DC characteristics

Figure 2 shows the I_d-V_g curves of TFTs with 12 nm, 22 nm and 45 nm gate oxides. Good switching characteristics were obtained in 3 devices. The drain current increased with the decrease in gate oxide thickness. Figure 3 shows the threshold voltage and the subthreshold slopes of TFTs with various channel lengths. Note that in the case of 12 nm gate oxide TFTs, the excellent subthreshold slope value of about 60 mV/decade was obtained in less than 2 μm channel length devices. Although threshold voltage became lower with channel length reduction in the thicker oxide TFTs, they had good cut-off characteristics, as shown in Fig. 2.

Analog gain

Figure 4 shows the I_d-V_g characteristics of 2 μm channel length TFT with 12 nm gate oxide. Figure 5 shows the gate oxide thickness dependence of output resistance (R_{out}) and intrinsic gain (R_{out}*g_m). Supply voltage was 5 V. The R_{out} values were degraded with reducing gate oxide thickness, while the R_{out}*g_m values were improved. Due to their small mobility compared with that of Si MOSFETs, the R_{out}*g_m values themselves were not so high, but the dependency to gate oxide thickness was similar to that of Si MOSFETs.

It was also confirmed that the transconductance efficiency (g_m/I_d) was improved in the TFTs with thinner gate oxide at the low gate overdrive voltage (V_{od}; V_g-V_t) of less than 0.5 V, as shown in Fig. 6. The values of 7.5 and 2.0 were obtained in 12 nm gate oxide TFTs at V_{od} = 0.2 V and 1.0 V, respectively, which were comparable to those of Si MOSFETs.

Figure 7 shows the gain of an amplifier transistor in a source follower circuit. The slope, the ratio of source voltage to gate voltage (dV_s/dV_g), corresponds to its gain. Almost ideal unity-gain was obtained in all TFTs, because substrate bias is not applied in the structure.

Flicker noise characteristics

Figure 8 shows the frequency dependence of input-referred spectral noise density (S_{Vg}) in the TFTs with 12 nm, 22 nm and 45 nm gate oxides. Supply voltage was 5 V. It was confirmed that the S_{Vg} decreased in inverse proportion to frequency. In addition, S_{Vg} values were approximately equal in the temperature range from RT to 120°C, as shown in Fig. 9. They were extrapolated at 1 Hz, and normalized by each channel area. Figure 10 shows the gate oxide thickness dependence of normalized S_{Vg} values at RT. It was found that they decreased in proportion to the square of gate oxide thickness even in TFTs. The results suggest that the noise in TFTs is mainly caused by carrier number fluctuation [4].

Figure 11 shows the dependence of normalized S_{Vg} values on gate overdrive voltage (V_{od}; V_g-V_t) in the TFTs. In the case of long channel TFTs (L_g=10μm), the S_{vg} values were almost the same in the wide gate bias range. In the case of short channel TFTs (L_g=1μm), S_{vg} values slightly degraded in the low V_{od} region, and improved with higher V_{od} bias condition.

The current density at low and high V_{od} was analyzed using the 2D Silvaco simulator ATLAS^{TM} [5], as shown in Fig. 12. Switching behavior and threshold voltage lowering in short channel devices were taken into consideration. At low V_{od} condition, electrons flow uniformly in an InGaZnO layer due to small vertical electric field at channel (Fig. 12 (a)). On the other hand, channel is formed only at the side of gate dielectrics at high V_{od} condition. Few electrons are observed at the other side (Fig. 12(b)).

The noise degradation was also analyzed using TFTs with back gate electrode. The molybdenum electrode was formed upper the channel, as shown in the insert figure of Fig. 13. In order to evaluate the noise behavior more correctly, the thicker gate oxide device was used. Figure 13 shows the I_d-V_g characteristics under back gate bias (V_{bg}) conditions. The V_t values were shifted lower and higher with positive V_{bg} and negative V_{bg}, respectively. The normalized S_{vg} values were degraded in positive V_{bg} condition and they were improved in negative V_{bg} condition, as shown in Fig. 14. The changes were large at low V_{od} and became small at higher V_{od}.

Figure 15 shows the 2D simulated results of current density in a TFT with back gate electrode. Even at low V_{od}, electrons flow avoiding back surface in the case under negative V_{bg} (Fig. 15(a)). In the case of positive V_{bg} and high V_{od}, electrons flow in the channels formed at both sides (Fig. 15(b)). A more accurate analysis is required, but it was found that the flicker noise characteristics of InGaZnO-TFTs are sensitive to the trap sites of back channel and strongly dependent on threshold voltage and overdrive voltage as shown in Fig. 16.

Conclusion

The analog characteristics of InGaZnO-TFTs with gate oxides between 12 nm and 45 nm have been investigated. It was confirmed that intrinsic gain (R_{out}*g_m) and transconductance efficiency (g_m/I_d) are improved with reducing gate oxide thickness. In a source follower circuit, almost ideal unity-gain (dV_s/dV_g) was obtained because substrate bias is not applied in the structure. Flicker noise characteristics were also improved with gate oxide thickness reduction. It was confirmed that the noise occurs mainly by carrier number fluctuation. In addition, it was found that flicker noise in low gate bias region is not negligible in the thick gate oxide case. They are strongly dependent on threshold voltage, gate overdrive voltage and the back interface quality. It was clarified that in InGaZnO-TFTs, taking the advantage of thinning the gate insulators is very important for achieving both high gain and low noise in analog applications.

References

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[2] K.Nomura et al., Nature 432, 488 (2004).
[3] K.Kato et al., JJAP, vol. 51, no. 2, pp. 021201 (2012).
[4] H.Mikoshiba, IEEE ED vol. 29, pp965-970 (1982).
[5] ATLAS Device Simulator, Silvaco

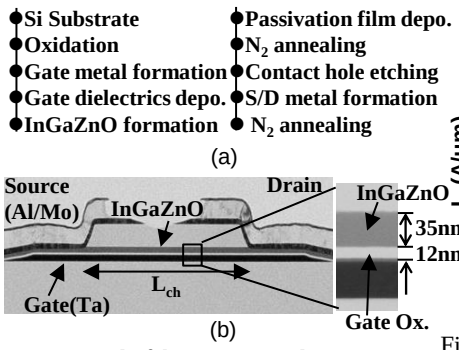

Fig. 1 Sample fabrication condition
(a) Fabrication process flow
(b) TEM cross section of an InGaZnO-TFT with 1 μm channel length.

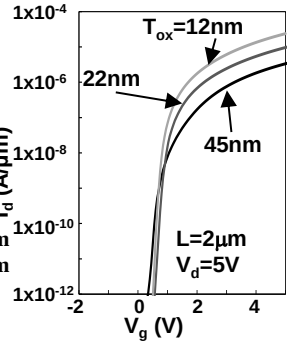

Fig. 2 I_d-V_g characteristics of TFTs with 2 μm channel length. Gate oxides are 12 nm, 22 nm and 45 nm.

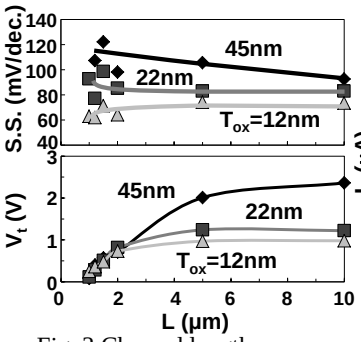

Fig. 3 Channel length dependence of subthreshold slope and threshold voltage in TFTs. Drain voltage is 5 V.

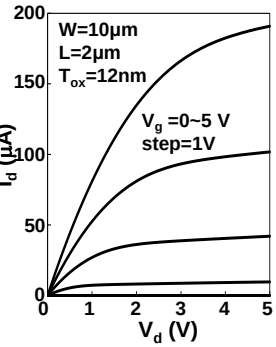

Fig. 4 I_d-V_d characteristics of 2 μm channel length TFT. Gate oxide thickness is 12 nm.

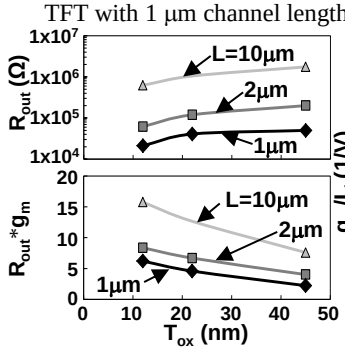

Fig. 5 Gate oxide thickness dependence of output resistance (R_{out}) and intrinsic gain (R_{out}*g_m) in TFTs.

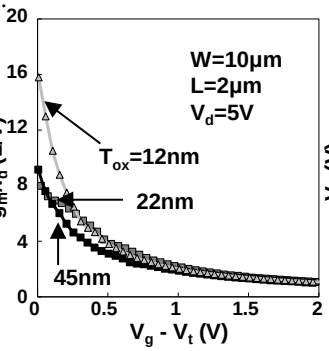

Fig. 6 Transconductance efficiency (g_m/I_d) of TFTs. Channel length is 2μm.

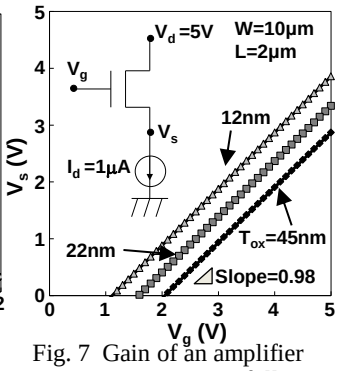

Fig. 7 Gain of an amplifier transistor in a source follower circuit. The slope, dV_s/dV_g, corresponds to its gain.

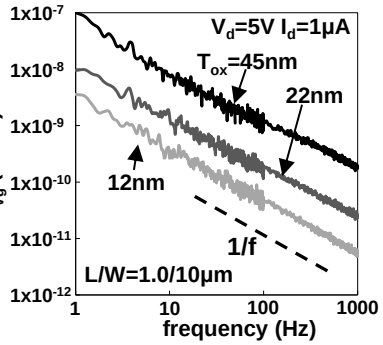

Fig. 8 1/f noise characteristics of TFTs. S_{Vg} decreased in inverse proportion to frequency.

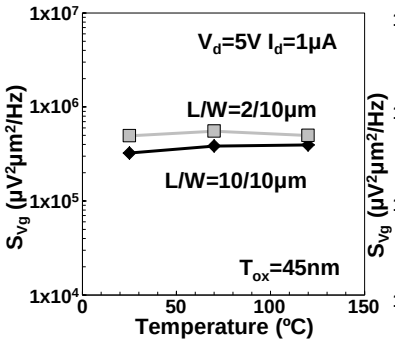

Fig. 9 Temperature dependence of normalized S_{Vg} in TFTs with 45 nm gate oxide.

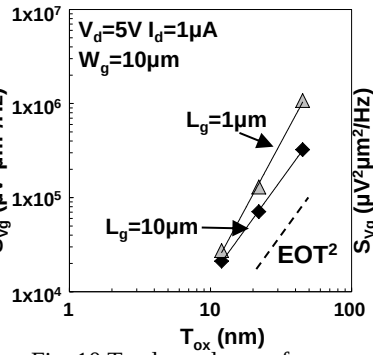

Fig. 10 T_{ox} dependence of normalized S_{Vg} in TFTs. In the case of L=10μm, S_{Vg} values decrease in proportion to square of T_{ox}.

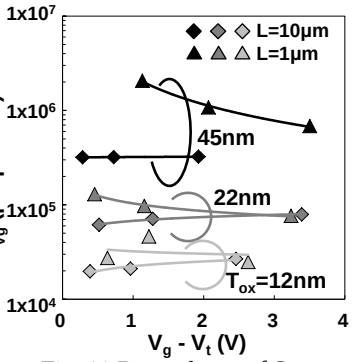

Fig. 11 Dependence of S_{Vg} on overdrive voltage in TFTs. Drain voltage is 5V.

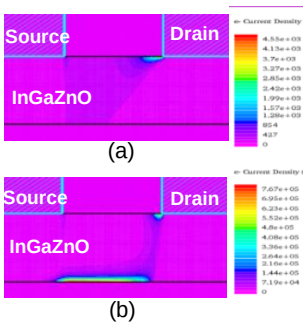

Fig. 12 Simulated current density in a TFT (a) Under low overdrive voltage condition (b) Under high overdrive voltage condition.

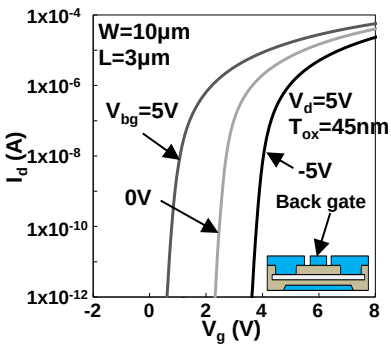

Fig. 13 I_d-V_g characteristics of a TFT with back gate electrode. V_t shits occurred under back gate negative bias (-5V) and positive bias (5V).

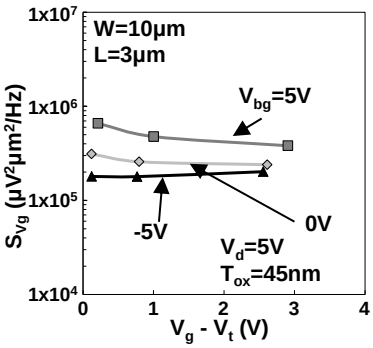

Fig. 14 Dependence of S_{Vg} on V_g-V_t in TFTs under back gate bias conditions.

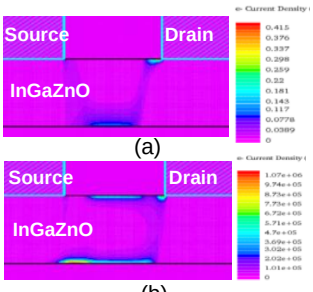

Fig. 15 Simulated current density in a TFT (a) Under low overdrive voltage and negative V_{bg} condition (b) Under high overdrive voltage and positive V_{bg} condition.

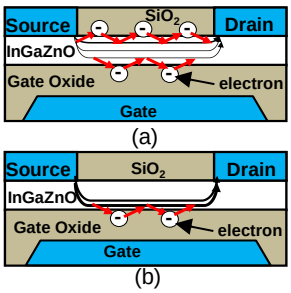

Fig. 16 Current flow and interface carrier trapping of TFTs (a) Large S_{Vg} case under low overdrive voltage condition (b) Low S_{Vg} case under high overdrive voltage condition.