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Fabrication and Characterization of High-Performance ZnO Thin-Film Transistors

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Abstract

A novel process which is capable of simultaneously forming the thin channel and S/D metal contacts of a sub-micron ZnO thin-film transistor was proposed and demonstrated in this work. In addition of the superior device characteristics, very small variation among the devices with the same channel dimensions is also verified.

1. Introduction

Metal oxide semiconductors have attracted much attention in recent years due to their low-temperature fabrication and superior properties like high electron mobility and high transparency [1] [2]. Recently, integration of thin-film transistors (TFTs) with metal-oxide as the channel material in the BEOL process of CMOS chips has been proved to be feasible [3][4]. In this study, we proposed a new method modified from the previous work [5] to fabricate ZnO TFTs with self-assembled channel. In the previous study [5], a metal shadow mask was utilized to make the ITO coplanar homojunction TFTs. The shadow mask features a pair of holes to define the source and drain (S/D) regions, respectively, and a "self-assembled" ITO channel was formed simultaneously by the sputtering of an ITO film. Although this method is simple, a few issues restrict its application in practical circuit manufacturing. First, the device dimensions are usually in tens of micrometers and hard to be scaled further because of the use of the metal shadow mask. Second, poor uniformity in device characteristics originating from the bending of the shadow mask is expected. Furthermore, the lack of S/D metal contacts in the fabricated devices results in high series resistance. In this work, to overcome the aforementioned shortcomings, a new approach utilizing mature photolithography and etch techniques is developed.

2. Experimental Details

This approach was demonstrated with a simple one-mask process depicted in Fig.1, in which the Si substrate was used as the bottom gate for simplicity. Unlike the previous work [5] which employed an ITO as the channel layer, in this work a ZnO film was deposited. First, 400nm-thick SiO_2 and 200nm-thick poly-Si were deposited by LPCVD. After a photolithographic step with an i-line stepper to define the S/D regions, the top poly-Si was etched by a plasma etcher, followed by a selective wet etching to remove the underlying SiO_2. Due to the isotropic etching, a suspending poly-Si bridge was formed and would serve as the shadow mask in the following steps. A 50nm-thick SiO_2 was subsequently deposited by PECVD as the gate dielectric. Then a ZnO film was deposited by rf sputtering under a pressure of 5mtorr at room temperature. During this step, a self-assembled ZnO channel was formed between the source and drain because of the scattering of the sputtering species taking place in the chamber. Finally, 100nm-thick Al film was deposited by thermal coater to form the self-aligned S/D contacts. Note that the deposited Al is disconnected between the source and drain owing to the ultra-low deposition pressure (~10^{-5} torr). The electrical characteristics of the fabricated ZnO TFTs were analyzed by an HP4156 system while the device structures were investigated by transmission electron microscopy (TEM).

3. Results and Discussion

Figs. 2a and 2b are the TEM images of the fabricated ZnO devices with channel length (L) of 0.4μm and 1μm, respectively. From the images, it can be seen clearly that a poly-Si bridge (the shadow mask) is suspending above the ZnO channel. Both ZnO and gate oxide are getting thinner toward the center of the channel. In addition, two Al pads are found to isolate from each other and form the S/D contacts. The differences in the film profile of ZnO, SiO_2 and Al are mainly attributed to the different deposition pressure of each material. Relatively high process pressure over the range of mtorr for ZnO and SiO_2 allows more significant scattering in the ambient and thus forming continuous film under the bridge. In contrast, Al is deposited by thermal coater with a working pressure of about 10^{-5} torr. Such low pressure results in negligible scattering in the chamber and forms isolated Al pads. Figs. 2c and 2d show the thinnest part of ZnO and SiO_2 at the center of channel. Thickness of ZnO and SiO_2 is 8.2nm and 14.5nm, respectively, for the device with L of 0.4μm, and decreases to 5.5nm and 7.6nm, respectively, for the one with L of 1μm. The thinning in the deposited films with increasing L is attributed to the less scattered species presenting under the longer bridge.

Transfer curves of the devices measured at V_D=0.1V and 3V are shown in Figs. 3a and 3b. Superior electrical characteristics with high on current and large on/off ratio (>10^9) are obtained. The high on current is partly due to the presence of Al S/D contacts. Subthreshold slopes evaluated from the curves under V_D=0.1V are 187mV/dec for the 0.4μm device and 71mV/dec for the 1μm one. The fabricated devices also demonstrate very high field-effect mobility (45.4cm^2/V-s as L= 0.4μm and 20.3cm^2/V-s as L= 1μm). To verify the variation of the fabricated devices, data measured from devices distributed in five different dies are exhibited in Figs. 3c and 3b. The results confirm the good uniformity of the developed process. Fig. 4 shows the comparison of the transfer curves between devices with different length. Devices with L= 0.4μm have more nega-

tive turn-on voltage and higher on current, which is attributed to the thicker ZnO channel and SiO_2 dielectric at the channel center.

4. Conclusion

A new process was developed to fabricate ZnO TFTs featuring self-assembled channel, self-aligned S/D contacts and sub-micron channel length. This new approach is effective to address the issues encountered in the previous work [5]. The fabricated devices also show excellent electrical characteristics including very high on/off current ratio (>10^9), high mobility (26~45 cm^2/V-s), steep subthreshold slope (71~187mV/dec), and good uniformity. The above results evidence the feasibility of this approach in the manufacturing of flat-panel displays and circuits embedded in the BEOL process of ICs.

References

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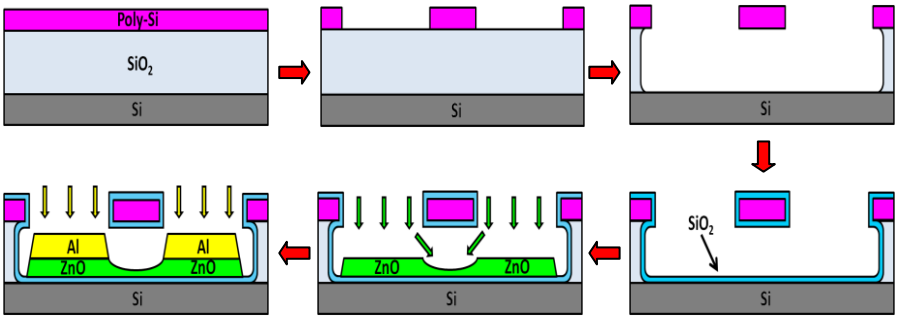

Fig. 1 Process flow of the proposed ZnO TFT. The deposited ZnO and Al on the top of the poly-Si are not shown in the last two steps for simplicity.

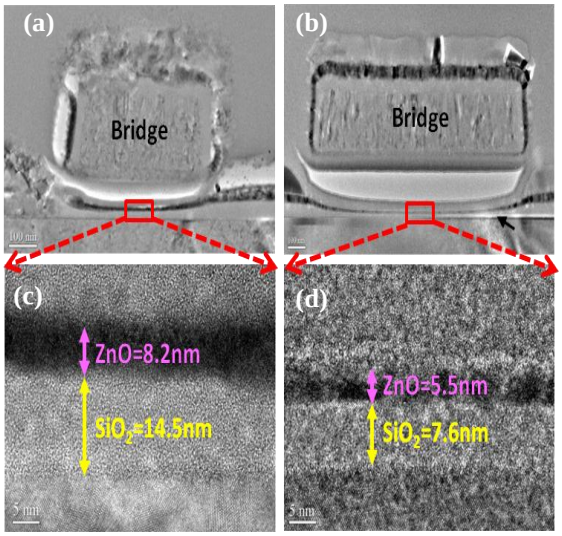

Fig. 2 Cross-sectional TEM images of ZnO devices with L of (a) 0.4μm and (b) 1μm. (c) and (d) show the enlarged views of the channel center.

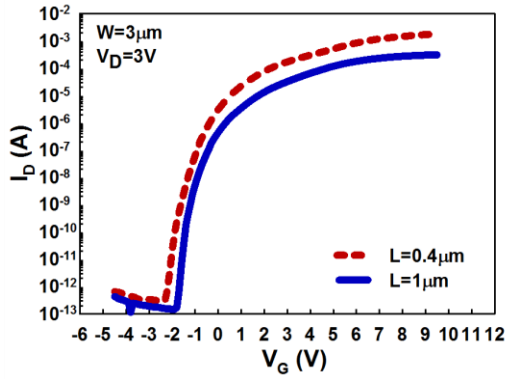

Fig. 4 Comparison of the transfer curves between devices with L = 0.4μm and 1μm.

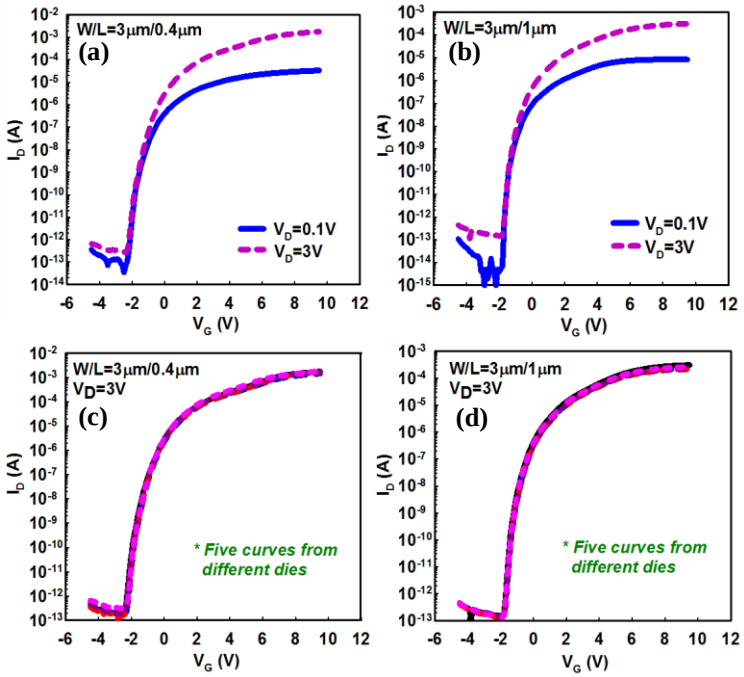

Fig. 3 Transfer characteristics measured at V_D=0.1V and V_D=3V for ZnO TFTs with L of (a) 0.4μm and (b) 1μm. (c) and (d) show five curves measured from devices with L of 0.4μm and 1μm, respectively, located in different dies.

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